UltraScale Architecture SelectIO Resources

Advance Specification User Guide

UG571 (v1.2) August 18, 2014

XILINX
ALL PROGRAMMABLE™

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
08/18/2014	1.2	Clarified sections of the SelectIO Resources Introduction and the IBUF_ANALOG description under SelectIO Primitives. Removed RTT_NONE from some possible values for ODT for split-termination DCI on page 24 and page 28. Added Note 1 to Table 1-11. Updated the description under HSUL_12 and DIFF_HSUL_12. Revised the HSUL_12 ODT description in Table 1-47. Moved Table 1-51 and Table 1-52. Added Note 3 to Table 1-54. Updated REFCLK_FREQUENCY in Table 2-2. Updated REFCLK in Table 2-3. Revised the DDR modes in Table 2-6. Updated REFCLK_FREQUENCY in Table 2-10. Removed the DDR 2:1 ratio in Table 2-13. In Table 2-17, updated CTRL_CLK. Updated REFCLK_FREQUENCY in Table 2-20.
05/08/2014	1.1	Added features to Table 1-1 and Note 3. Revised the Differences from Previous Generations section. Added clarification to various sections with regards to the OUTPUT_IMPEDANCE attribute. Updated the default for the DCIUpdateMode option to ASREQUIRED. An example discussion added below Table 1-9. Removed V_{REF} tuning from the IBUFDSE3 and IOBUFDSE3 primitives. Added IBUF_ANALOG, IOBUF_INTERMDISABLE, and IBUFDS_DIFF_OUT_INTERMDISABLE to SelectIO Primitives, page 35. Throughout Chapter 1, removed IBUFG (clock input buffer) and updated Figure 1-18, removed IBUFGDS (differential clock input buffer) and updated Figure 1-22, and removed IBUFGDS_DIFF_OUT (differential clock input buffer with complementary outputs) and updated Figure 1-23. Updated the descriptions and some figures and tables: IBUF_IBUFDISABLE, IBUF_INTERMDISABLE, IBUFE3, IBUFDS_DIFF_OUT_IBUFDISABLE, IBUFDS_IBUFDISABLE, IBUFDS_INTERMDISABLE, IBUFDSE3, IOBUF_DCIEN, IOBUFE3, IOBUFDS, IOBUFDS_DCIEN, IOBUFDS_DIFF_OUT, IOBUFDS_DIFF_OUT_DCIEN, IOBUFDS_INTERMDISABLE, IOBUFDS_DIFF_OUT_INTERMDISABLE, IOBUFDSE3, HPIO_VREF, IBUF_LOW_PWR Attribute, Output Slew Rate Attributes, Differential Termination Attribute, Internal V_{REF}, DQS_BIAS, Transmitter Pre-Emphasis, LVDS Transmitter Pre-Emphasis, Receiver EQUALIZATION, LVDCI (Low-Voltage Digitally Controlled Impedance), HSLVDCI (High-Speed LVDCI), HSTL (High-Speed Transceiver Logic), Table 1-48, Table 1-49, Table 1-51, Table 1-52, Table 1-55, and Figure 1-81. Added IBUFDS_DIFF_OUT_IBUFDISABLE, IOBUF_INTERMDISABLE, Source Termination Attribute (OUTPUT_IMPEDANCE), Table 1-12, Table 1-13, and VREF_CNTR. Added the MEDIUM attribute to the HP I/O bank primitives in Table 1-19, Table 1-20, Table 1-21, Table 1-23, Table 1-35, Table 1-36, Table 1-43, Table 1-44, Table 1-47, Table 1-50, and Table 1-73. Updated columns in Table 1-54. Added clarifications to the DQS_BIAS discussion on page 121. Removed SUB_LVDS_25 and replaced with SUB_LVDS on page 126 and throughout the remaining tables including Table A-1. Removed attributes from Table 1-71. Updated the discussion in Rules for Combining I/O Standards in the Same Bank. Added Note 3 and Note 4 to Table 1-72. Added Note 5 to Table 1-73. See Chapter 2 revisions on next page.

Date	Version	Revision
05/07/2014	1.1 (continued)	Updated Figure 2-2. Updated the Input Delay and Output Delay discussions. Updated Table 2-3 and Table 2-4. In Table 2-2, Table 2-10, Table 2-20, and Table 2-22, clarified descriptions for DELAY_VALUE (DELAY_VALUE_EXT), DELAY_FORMAT, and UPDATE_MODE. In Table 2-8, updated the DATA_WIDTH description. Updated the SerDes Output Data Bits to Use in Table 2-6. Added Type column to Table 2-10 and Table 2-12. In Table 2-16, updated the RIU_VALID port description and the port widths and descriptions for the BIT_CTRL ports. In Table 2-17, updated the SERIAL_MODE description, the READ_IDLE_COUNT[5:0] default value, the ROUNDING_FACTOR type, CTRL_CLK, and added new attributes: SELF_CALIBRATE, IDLY_VT_TRACK, ODLY_VT_TRACK, QDLY_VT_TRACK, and RXGATE_EXTEND. Updated Figure 2-14. Removed the CLK_OUT port from Table 2-19 and updated RX_BIT_CTRL_IN<39:0>, through TX_BIT_CTRL_OUT<39:0>. In Table 2-20, updated values for DELAY_VALUE, REFCLK_FREQUENCY, DATA_WIDTH, and added the UPDATE_MODE_EXT attribute. Updated Figure 2-16. In Table 2-21, updated the BITSLICE_CONTROL ports. Table 2-22, updated values for DELAY_VALUE, REFCLK_FREQUENCY, and added the ENABLE_PRE_ EMPHASIS attribute.
12/10/2013	1.0	Initial Xilinx release.

Table of Contents

SelectIO Resources

Introduction to the UltraScale Architecture

The Xilinx® UltraScale™ architecture is a revolutionary approach to creating programmable devices capable of addressing the massive I/O and memory bandwidth requirements of next generation applications while efficiently routing and processing the data brought on-chip. UltraScale devices address a vast spectrum of high-bandwidth, high-utilization system requirements through industry-leading technical innovations. UltraScale architecture-based devices share many building blocks to provide optimized scalability across the product range, as well as numerous new power reduction features for low total power consumption.

Kintex® UltraScale FPGAs provide high performance with a focus on optimized performance per watt for applications including wireless, wired, and signal or image processing. High DSP and block RAM-to-logic ratios, and next generation transceivers are combined with low-cost packaging to enable an optimum blend of capability for these applications.

Virtex® UltraScale FPGAs provide the highest system capacity, bandwidth, and performance. Delivering unprecedented logic capacity, serial I/O bandwidth, and on-chip memory, the Virtex UltraScale family pushes the performance envelope ever higher.

This user guide describes the UltraScale architecture SelectIO™ resources and is part of the UltraScale Architecture documentation suite available at: www.xilinx.com/ultrascale.

I/O Tile Overview

Input/output characteristics and logic resources are covered in two consecutive chapters.

Chapter 1, SelectIO Resources describes the electrical behavior of the output drivers and input receivers, and gives detailed examples of many standard interfaces.

Chapter 2, SelectIO Logic Resources describes the I/O logic resources available.

The UltraScale devices offer both high-performance (HP) and high-range (HR) I/O banks. The HP I/O banks are designed to meet the performance requirements of high-speed memory and other chip-to-chip interfaces with voltages up to 1.8V. The HR I/O banks are designed to support a wider range of I/O standards with voltages up to 3.3V. Table 1-1 highlights the features supported in the HP and HR I/O banks. See Table 1-1 for help when making initial decisions on I/O banks for particular design requirements. See the specific UltraScale device data sheet [Ref 1] for details on the performance and other electrical requirements of the HP and HR I/O banks.

The UltraScale devices contain different combinations of HR and HP I/O banks. The *UltraScale Architecture and Product Overview* (DS890) [Ref 2] documents the available number of each type of bank for all devices.

Table 1-1: **Supported Features in the HR and HP I/O Banks**

Feature	HP I/O Banks	HR I/O Banks
3.3V I/O standards(1)	N/A	Supported
2.5V I/O standards(1)	N/A	Supported
1.8V I/O standards(1)	Supported	Supported
1.5V I/O standards(1)	Supported	Supported
1.35V I/O standards(1)	Supported	Supported
1.2V I/O standards(1)	Supported	Supported
1.0V POD I/O standard	Supported	N/A
LVDS signaling	Supported(2)	Supported
Digitally-controlled impedance (DCI) and DCI cascading	Supported	N/A
Internal V_{REF}	Supported	Supported
Internal differential termination (DIFF_TERM)	Supported	Supported
IDELAY	Supported	Supported
ODELAY	Supported	Supported
IDELAYCTRL	Supported	Supported
ISERDES	Supported	Supported
OSERDES	Supported	Supported
Transmitter pre-emphasis	Supported	Supported(3)
Receiver equalization	Supported	Supported
Receiver offset control	Supported	Not supported
Receiver V_{REF} scan	Supported	Not supported

Notes:

1. The I/O Bank Type column in Table 1-73 shows the specific I/O standards that are available in the HP and HR I/O banks.
2. Although LVDS is generally considered a 2.5V I/O standard, it is supported in both the HR and HP I/O banks.
3. Only LVDS pre-emphasis is supported in HR I/O banks.

Differences from Previous Generations

UltraScale devices support many of the same features supported in 7 series devices. However, there are some useful new features, along with changes to several existing features. These new features and changes include:

- Each I/O bank contains 52 SelectIO pins. In some devices, there are some HR I/O mini-banks containing 26 SelectIO pins, each with their own independent power supply and V_{REF} pin.

TIP: *All references in this user guide discussing HR I/O banks also apply to HR I/O mini-banks.*

- Support for pseudo-open-drain logic standards (POD).
- Series output termination control is available in HP I/O banks for improved signal integrity and ease of board design.
- Internal V_{REF} level scan (HP I/O banks only). One dedicated external V_{REF} pin per bank.
- Pre-emphasis is available for the DDR4 standard in HP I/O banks and the LVDS TX standard in HP/HR I/O banks. Pre-emphasis reduces inter-symbol interference and minimizes the effects of transmission line losses.
- Linear equalization on V_{REF}-based receivers (in HP I/O banks) and differential receivers (in both HP and HR I/O banks) is available to overcome high-frequency losses through the transmission channel.
- Receiver offset cancellation is available for some I/O standards to compensate for process variations (HP I/O banks only).
- Digitally controlled impedance (DCI) is only available in HP I/O banks. DCI uses only one reference resistor per bank, 240Ω to GND on the VRP pin. The value of the driver or input termination are determined by the OUTPUT_IMPEDANCE and ODT attributes, respectively.
- V_{CCAUX_IO} only supports a nominal voltage level of 1.8V.
- A SLEW value of *MEDIUM* is supported in HP I/O banks.
- The DCITERMDISABLE port can control both DCI and non-DCI on-die input termination features in HP I/O banks.
- Where applicable, asserting IBUFDISABLE causes the input to the interconnect logic to be a 0. This is different from the resulting 1 after asserting IBUFDISABLE in 7 series devices.
- The BITSLICE is effectively a physical layer (PHY) block that replaces and enhances the functionality of the component mode primitives. This PHY block gives tighter control over timing and provides new features enabling higher data rate reception in UltraScale

devices. See Input Using Native Mode in Chapter 2.

SelectIO Resources Introduction

All UltraScale devices have configurable SelectIO drivers and receivers, supporting a wide variety of standard interfaces. The robust feature set includes programmable control of output strength and slew rate, on-chip termination using digitally-controlled impedance (DCI), and the ability to internally generate a reference voltage (INTERNAL_VREF).

IMPORTANT: *HR I/O banks do not have DCI. Therefore, any reference to DCI in this user guide does not apply to the HR I/O banks.*

With some exceptions, each I/O bank contains 52 SelectIO pins, where 48 can implement both single-ended and differential I/O standards. The other four pins, including the multipurpose VRP pin, are single-ended (only) IOBs. Every SelectIO resource contains input, output, and 3-state drivers.

The SelectIO pins can be configured to various I/O standards, both single-ended and differential.

- Single-ended I/O standards (for example: LVCMOS, LVTTL, HSTL, SSTL, HSUL, and POD)
- Differential I/O standards (for example: LVDS, Mini_LVDS, RSDS, PPDS, BLVDS, TMDS, SLVS, LVPECL, SUB_LVDS, and differential HSTL, POD, HSUL, and SSTL)

When not used as a VRP pin, the multipurpose VRP pin in each bank can only be used with single-ended I/O standards. Figure 1-1 shows the single-ended (only) HP I/O block (IOB) and its connections to the internal logic and the device pad. Figure 1-2 shows the standard HP IOB. Figure 1-3 shows the single-ended (only) HR IOB. Figure 1-4 shows the standard HR IOB. Figure 1-5 shows the relative location of the single-ended IOBs within a bank. When not configured, I/O drivers are 3-stated and I/O receivers are weakly pulled-down.

Each IOB has a direct connection to BITSLICE components containing the input and output resources for serialization, deserialization, signal delay, clock, data, and 3-state control, and registering for the IOB. The BITSLICE components can be used in component mode individually as IDELAY, ODELAY, ISERDES, OSERDES, and input and output registers. They can also be used at a lower granularity level as RX_BITSLICE (input), TX_BITSLICE (output), and RXTX_BITSLICE (bidirectional) components where all of the BITSLICE functions are grouped together in a single interface. See Chapter 2, SelectIO Logic Resources for more information.

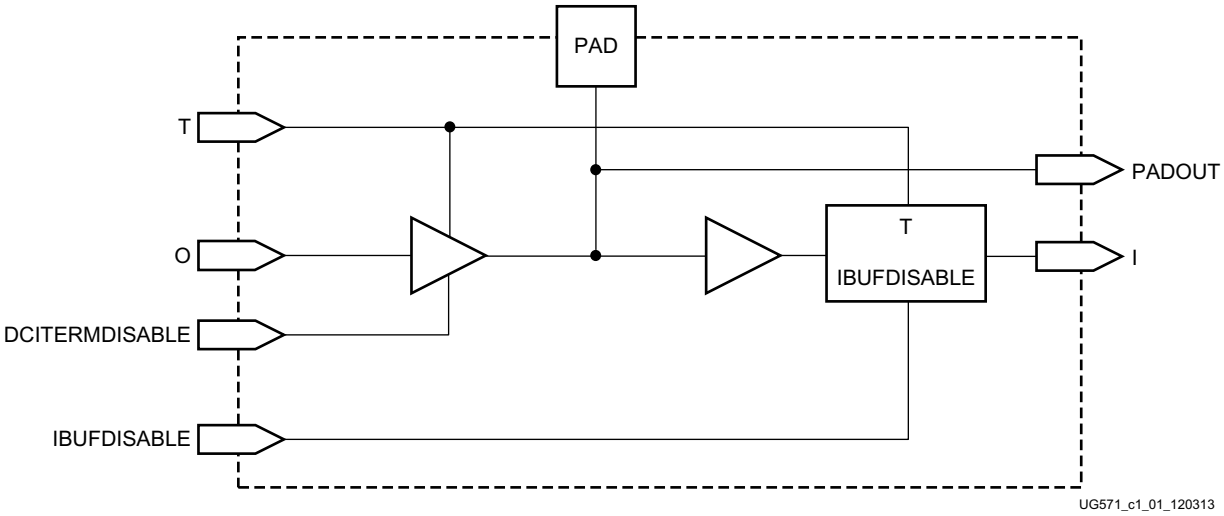

Figure 1-1: **Single-Ended (Only) HP IOB Diagram**

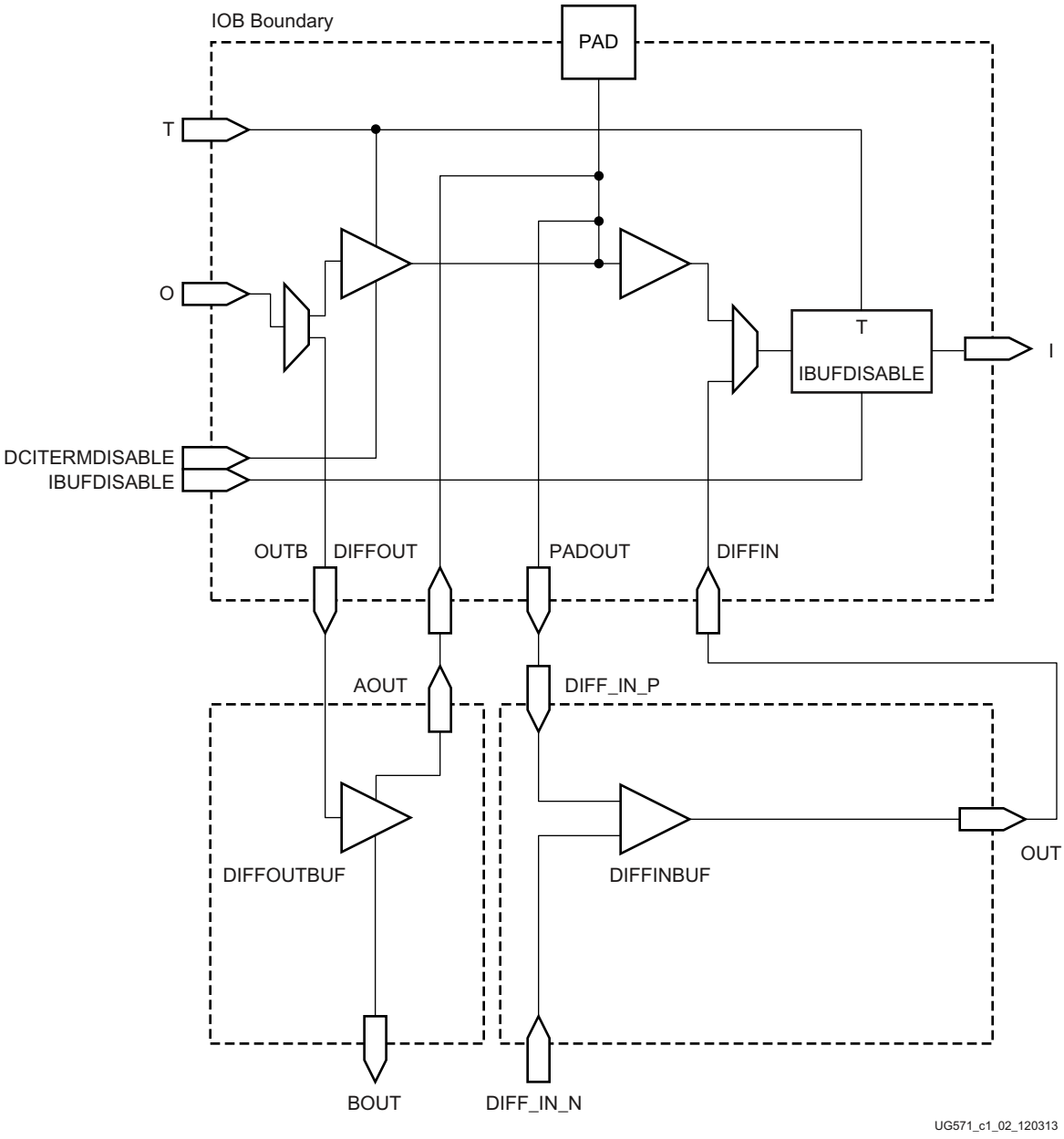

Figure 1-2: **Standard HP IOB Diagram**

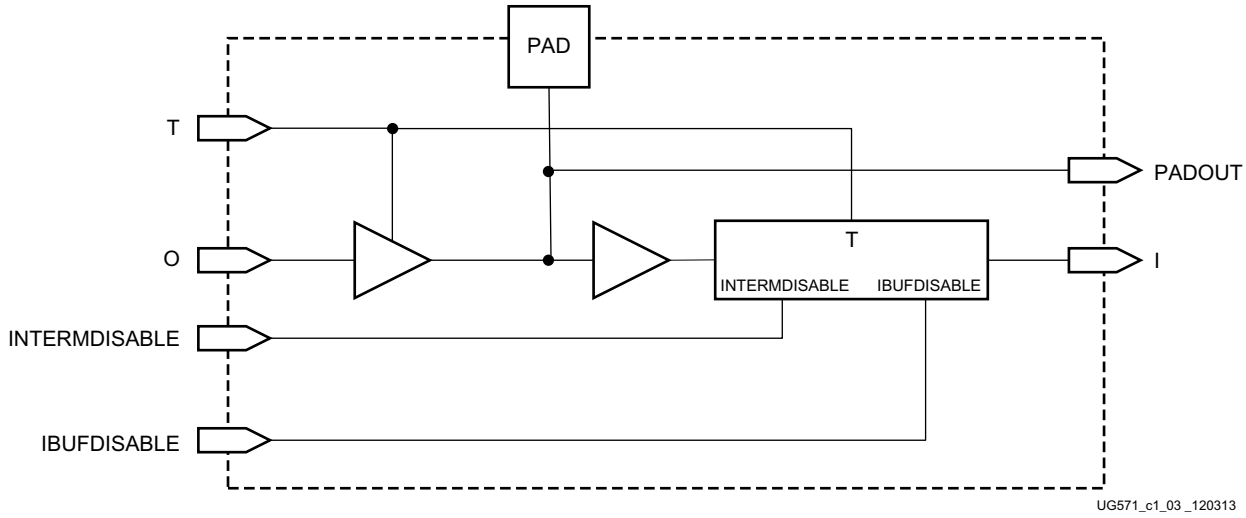

Figure 1-3: **Single-Ended (Only) HR IOB Diagram**

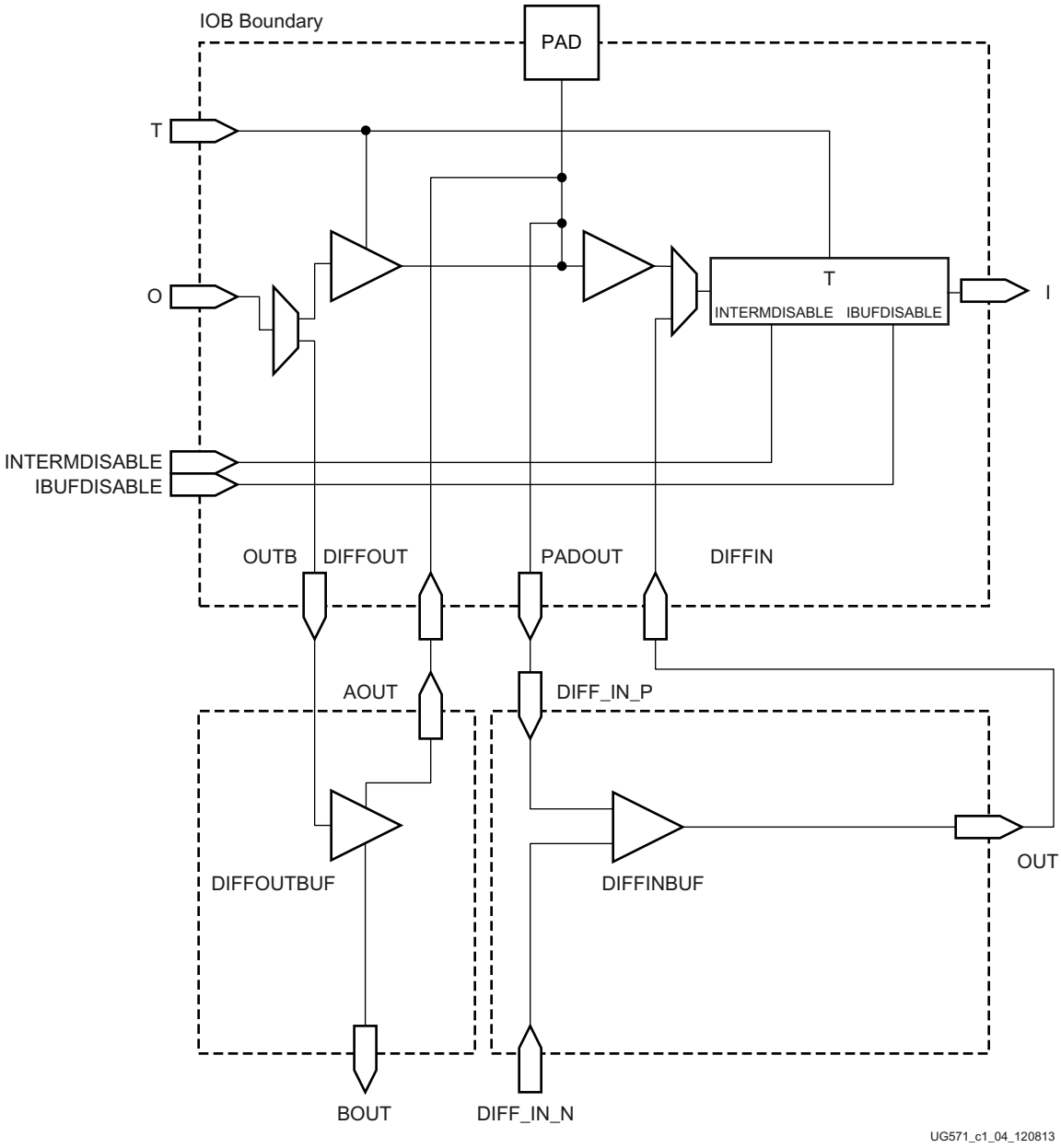

Figure 1-4: **Standard HR IOB Diagram**

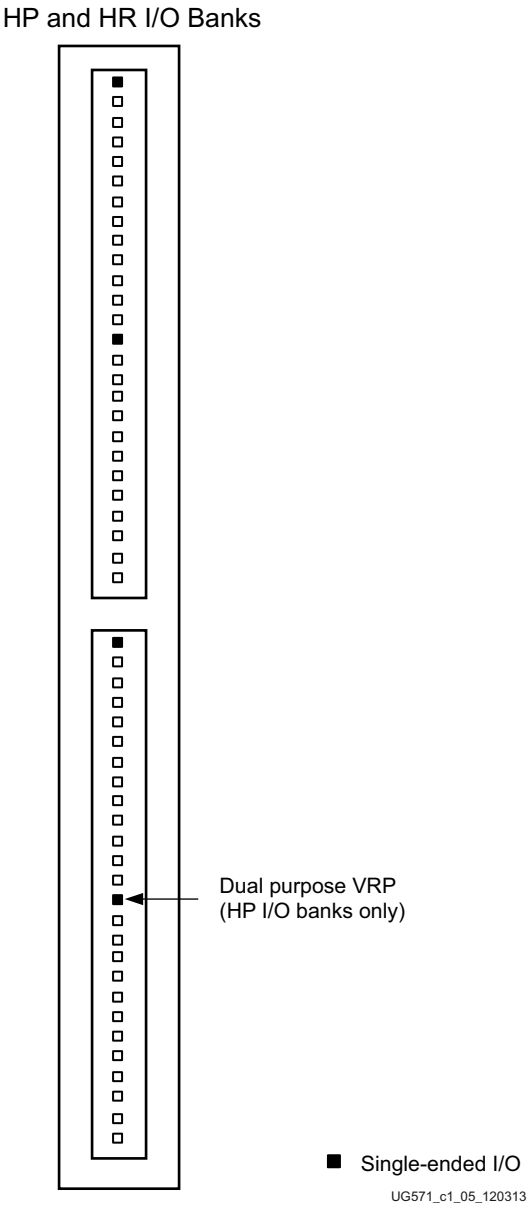

Figure 1-5: **Relative Single-ended I/O Locations within an HR or HP I/O bank**

SelectIO Resources General Guidelines

This section summarizes the general guidelines to be considered when designing with the SelectIO resources in UltraScale devices.

I/O Bank Rules

Most I/O banks consist of 52 IOBs, although HR I/O mini-banks consist of 26 IOBs. The number of banks depends upon the device size and the package pinout. In the *UltraScale Architecture and Product Overview* (DS890) [Ref 2] the total number of available I/O is listed by device type. Figure 1-6 is an example of a typical floorplan. The *UltraScale Architecture Packaging and Pinout Specifications* (UG575) [Ref 3] includes information on the I/O banks for each device/package combination.

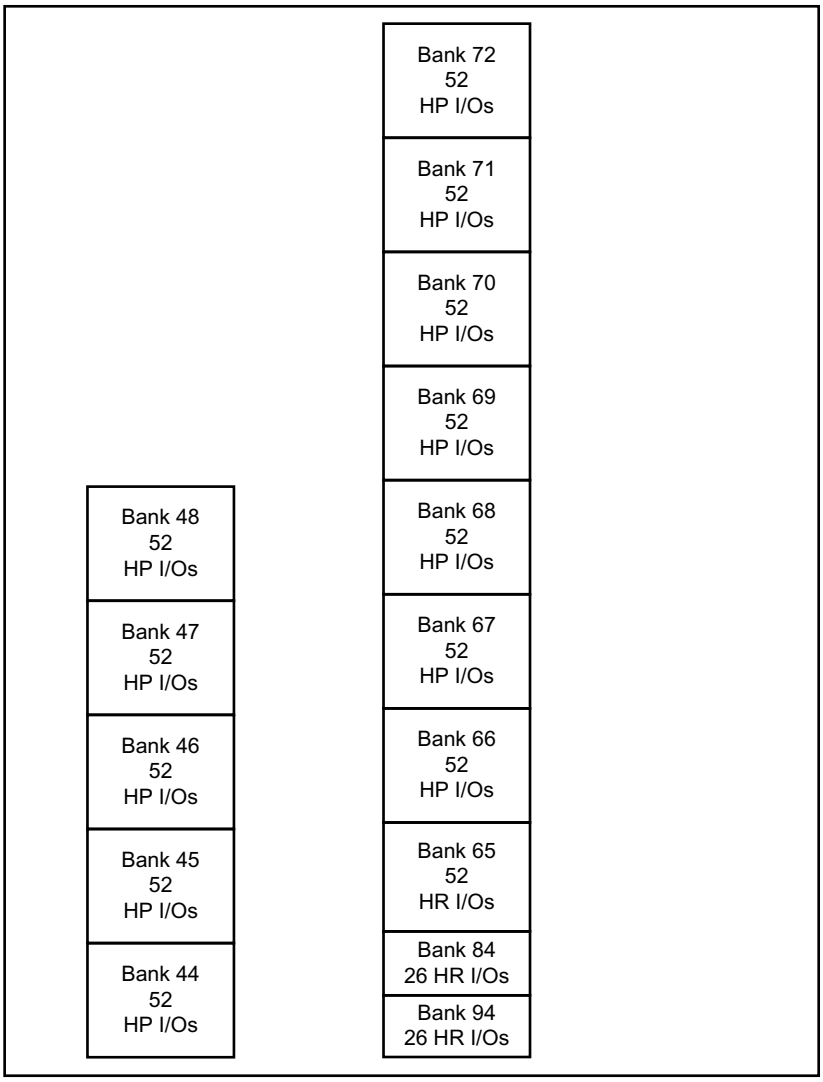

Figure 1-6: **Example I/O Banks**

Supply Voltages for the SelectIO Pins

V_{CCO}

The V_{CCO} supply is the primary power supply of the I/O circuitry. The V_{CCO} (V) columns in Table 1-72 provide the V_{CCO} requirements for each of the supported I/O standards, and illustrate the V_{CCO} requirements for inputs and outputs as well as the optional internal differential termination circuit. All V_{CCO} pins for a given HP I/O bank must be connected to the same external voltage supply on the board, and as a result, all of the I/O within a given I/O bank must share the same V_{CCO} level. The V_{CCO} voltage must match the requirements for the I/O standards that have been assigned to the I/O bank. Incorrect V_{CCO} voltages can result in loss of functionality or damage to the device.

V_{REF}

Single-ended I/O standards with a differential input buffer require an input reference voltage (V_{REF}). When V_{REF} is required within an I/O bank, the dedicated V_{REF} pin can be used as a V_{REF} supply input. An internally generated reference voltage is enabled by using the INTERNAL_VREF constraint. For more information on this constraint, see SelectIO Attributes/Constraints, page 54.

RECOMMENDED: *When not in use, the dedicated V_{REF} pin should be connected to GND.*

An internal V_{REF} scan feature is available in HP I/O banks to account for process variations and system considerations.

V_{CCAUX}

The global auxiliary (V_{CCAUX}) supply rail primarily provides power to the interconnect logic of the various blocks inside the device. In the I/O banks, V_{CCAUX} is also used to power input buffer circuits for some of the I/O standards. These include some of the single-ended I/O standards at or below 1.8V, and also some of the 2.5V standards (HR I/O banks only). Additionally, the V_{CCAUX} rail provides power to the differential input buffer circuits used for most of the differential and V_{REF} I/O standards.

The power supply requirements, including power-on and power-off sequencing, are described in the UltraScale device data sheets [Ref 1].

V_{CCAUX_IO}

The auxiliary I/O (V_{CCAUX_IO}) voltage supply rail provides power to the I/O circuitry. V_{CCAUX_IO} should only be powered by 1.8V.

V_{CCINT_IO}

This is an internal supply for I/O banks. Connect to the V_{CCINT} voltage supply rail.

DCI—Only available in the HP I/O Banks

Introduction

As device footprints increase and system clock speeds get faster, PC board design and manufacturing becomes more difficult. With ever faster edge rates, maintaining signal integrity becomes a critical issue. PC board traces must be properly terminated to avoid reflections or ringing.

To terminate a trace, resistors are traditionally added to make the output and/or input match the impedance of the receiver or driver to the impedance of the trace. However, due to increased device I/Os, adding resistors close to the device pins increases the board area and component count, and can in some cases be physically impossible. To address these issues and to achieve better signal integrity, Xilinx developed the digitally controlled impedance (DCI) technology.

Depending on the I/O standard, DCI can either control the output impedance of a driver, or add a parallel termination present at the receiver, with the goal of accurately matching the characteristic impedance of the transmission line. DCI actively adjusts these impedances inside the I/O to calibrate to an external precision reference resistor placed on the VRP pin. This compensates for changes in I/O impedance due to process variation. It also continuously adjusts the impedances to compensate for variations of temperature and supply voltage fluctuations.

IMPORTANT: *For all DCI I/O standards, the external reference resistor (R_{VRP}) should be 240Ω.*

For the I/O standards with controlled parallel termination, DCI provides the parallel termination for receivers. This eliminates the need for termination resistors on the board, reduces board routing difficulties and component count, and improves signal integrity by eliminating stub reflection. Stub reflection occurs when termination resistors are located too far from the end of the transmission line. With DCI, the termination resistors are as close as possible to the output driver or the input buffer, thus, eliminating stub reflections. The exact value of the termination resistors is determined by the ODT attribute for controlled parallel termination. The exact driver termination value is determined by the OUTPUT_IMPEDANCE attribute for the controlled impedance driver. DCI is only available in HP I/O banks. DCI is not available in HR I/O banks.

DCI uses one multipurpose reference VRP pin in each I/O bank to control the impedance of the driver or the parallel-termination value for all of the I/Os of that bank.

IMPORTANT: *When using DCI standards, the VRP pin must be terminated to GND by a reference resistor. The value of the resistor should be 240Ω.*

To implement DCI in a design:

1. Assign one of the DCI I/O standards in an HP I/O bank (see Table 1-3).
2. Connect the VRP multi-function pin to a precision resistor (240Ω) tied to GND.
3. Set the desired termination value using the ODT attribute for all applicable I/Os with controlled parallel terminations. Set the termination value using the OUTPUT_IMPEDANCE attribute for all applicable I/Os with a controlled impedance driver.

If several I/O banks in the same I/O bank column are using DCI, the internal VRP node can be cascaded so that only one VRP pin for all of the I/O banks in the entire I/O column is required to be connected to a precision resistor. This option is called DCI cascading as is detailed in DCI Cascading, page 20. This section also describes how to determine if I/O banks share the same I/O bank column. If DCI I/O standards are not used in the bank, the VRP pin is available as a standard I/O pin. The *UltraScale Architecture Packaging and Pinout Specifications* (UG575) [Ref 3] gives detailed pin descriptions.

DCI adjusts the impedance of the I/O by selectively turning resistors in the I/Os on or off. The adjustment starts during the device start-up sequence. By default, the DONE pin does not transition High until the first part of the impedance adjustment process is completed.

The DCI calibration can be reset by instantiating the DCIRESET primitive. Toggling the RST input to the DCIRESET primitive while the device is operating resets the DCI state machine and restarts the calibration process. All I/Os using DCI are unavailable until the LOCKED output from the DCIRESET block is asserted. This functionality is useful in applications where the temperature and/or supply voltage changes significantly from device power-up to the nominal operating condition.

For controlled impedance output drivers, the exact value of the driver terminations is determined by the OUTPUT_IMPEDANCE attribute. For the I/O standards that support parallel termination, DCI creates a Thevenin equivalent, or split-termination resistance to the $V_{CCO}/2$ voltage level, or a single-termination resistance to the V_{CCO} voltage level. The value of split-termination resistors are determined by the ODT attribute. For POD and HSUL standards, DCI supports single termination to V_{CCO}. The value of the termination resistance is determined by the ODT attribute.

Match_cycle Configuration Option

Match_cycle is a configuration option that can halt the start-up sequence at the end of the device configuration sequence until the DCI logic has performed the first match (calibration) to the external reference resistor. This option is also sometimes referred to as DCI match.

DCIUpdateMode Configuration Option

DCIUpdateMode is a configuration option that can override control of how often the DCI circuit updates the impedance matching to the VRP reference resistor. This option defaults to ASREQUIRED in the Xilinx implementation tools. The settings for the DCIUpdateMode configuration option are:

- **ASREQUIRED**: Initial impedance calibration is made at device initialization, and dynamic impedance adjustments are made as needed throughout device operation (default).
- **QUIET**: Impedance calibration is done once at device initialization, or each time the RST pin is asserted on the DCIRESET primitive for designs that include this primitive.

RECOMMENDED: *It is strongly recommended that the DCIUpdateMode option be kept with the default value of ASREQUIRED so that the DCI circuitry is allowed to operate normally.*

DCIRESET Primitive

DCIRESET is a Xilinx design primitive that provides the capability to perform a reset of the DCI controller state machine during normal operation of the design. This primitive is required in a design when DCIUpdateMode is set to QUIET (see DCIUpdateMode Configuration Option) or for the case outlined in Using DCI with the Multi-function Configuration Pins. See the *UltraScale Architecture Libraries Guide* (UG974) [Ref 6] for more details on the DCIRESET primitive.

Using DCI with the Multi-function Configuration Pins

UltraScale devices have pins dedicated to configuration functions contained in I/O Bank 0. There are also I/O pins in bank 65 known as multi-function or multipurpose pins that can also be used for configuration, but then convert to normal I/O pins after configuration is complete. If any of these multi-function pins in I/O bank 65 are assigned as DCI I/O standards (in devices where bank 65 is an HP I/O bank), you should also include and use the DCIRESET primitive in your design. In that case, the design should pulse the RST input of DCIRESET and then wait for the LOCKED signal to be asserted prior to using any multi-function pins input or outputs with DCI standards. This is required because the multi-function configuration I/O pins ignore the initial DCI calibration that happens during the normal device initialization because they must perform as configuration pins.

As a result, if the DCIRESET primitive had not been used and DCIUpdateMode was set to ASREQUIRED, after those pins become normal I/O pins there would be an indeterministic delay between the end of configuration and when the DCI calibration algorithm updated those pins DCI settings. If DCIRESET was not used and DCIUpdateMode was set to QUIET, these pins would never have their DCI values set. Including and using the DCIRESET primitive in the design allows the multi-function pins to have DCI I/O standards and to perform without issue.

DCI Cascading

The HP I/O banks using DCI I/O standards have the option of deriving the DCI impedance values from another HP I/O bank. As shown in Figure 1-7, a digital control bus is internally distributed throughout the bank to control the impedance of each I/O.

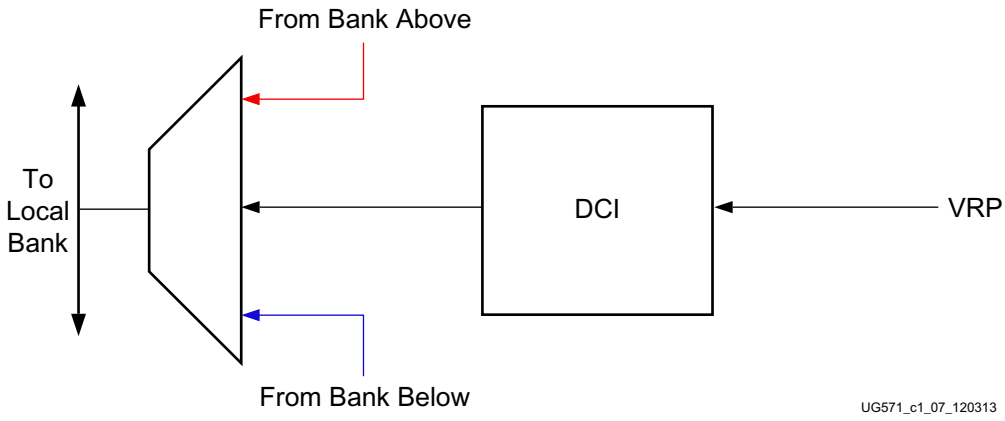

Figure 1-7: **DCI Use within a Bank**

With DCI cascading, one I/O bank (the master bank) must have its VRP pin connected to an external reference resistor. Other I/O banks in the same HP I/O bank column (slave banks) can use DCI standards with the same impedance as the master bank, without connecting the VRP pin on these slave banks to an external resistor. DCI impedance control in cascaded banks is received from the I/O master bank.

Figure 1-8 shows DCI cascading support over multiple I/O banks. Bank B is the master I/O bank, and Banks A and C are considered slave I/O banks.

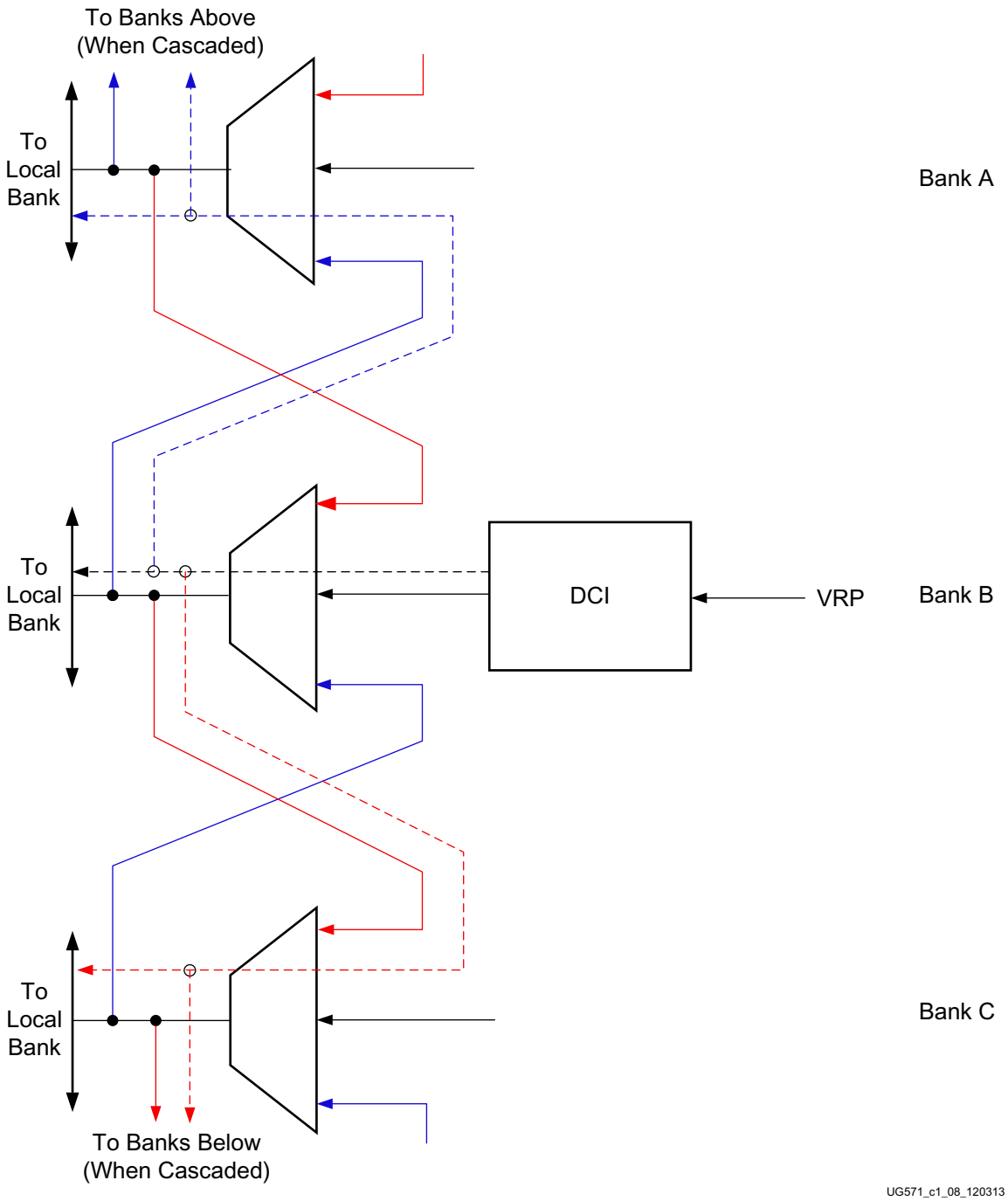

Figure 1-8: **DCI Cascading Supported Over Multiple I/O Banks**

The guidelines when using DCI cascading are as follows:

- DCI cascading is only available through a column of HP I/O banks
- The master and slave SelectIO banks must all reside on the same HP I/O column on the device and can span the entire column unless there is an interposer boundary.
- DCI cascading cannot pass through the interposer boundaries of the larger UltraScale devices with stacked silicon interconnect (SSI) technology.
- Master and slave I/O banks must have the same V_{CCO} and V_{REF} (if applicable) voltage.
- I/O banks in the same HP I/O column that are not using DCI (pass-through banks) do not have to comply with the V_{CCO} and V_{REF} voltage rules for combining DCI settings.
- DCI I/O banking compatibility rules must be satisfied across all master and slave banks.
- To locate I/O banks that reside in the same I/O column, see the figures in the *Die Level Bank Numbering Overview* section of the *UltraScale Architecture Packaging and Pinout Specifications* (UG575) [Ref 3].
- For specific information on implementing DCI cascading in a design, see DCI_CASCADE Constraint, page 54.

RECOMMENDED: *Unused banks must be powered up because leaving the V_{CCO} pins of unused I/O banks floating reduces the level of ESD protection on these pins and the I/O pins in the bank. If the bank is unpowered, DCI can still be cascaded through the unpowered bank.*

When DCI cascading is used, source and on-die input terminations have a bigger variation as compared to DCI used on a per bank basis without cascade.

Controlled Impedance Driver (Source Termination)

To optimize signal integrity for high-speed or high-performance applications, extra measures are required to match the output impedance of drivers to the impedance of the transmission lines and receivers. Optimally, drivers must have an output impedance matching the characteristic impedance of the driven line, otherwise reflections can occur due to discontinuities. To solve this issue, designers sometimes use external-source series-termination resistors placed close to the pins of high-strength, low-impedance drivers. The resistance values are chosen such that the sum of the output impedance of the driver plus the resistance of the source series-termination resistor roughly equals the impedance of the transmission line.

DCI can provide controlled impedance output drivers to eliminate reflections without requiring the use of an external source-termination resistor. The impedance is derived from the external reference resistor.

Figure 1-9 illustrates a controlled impedance driver inside a device.

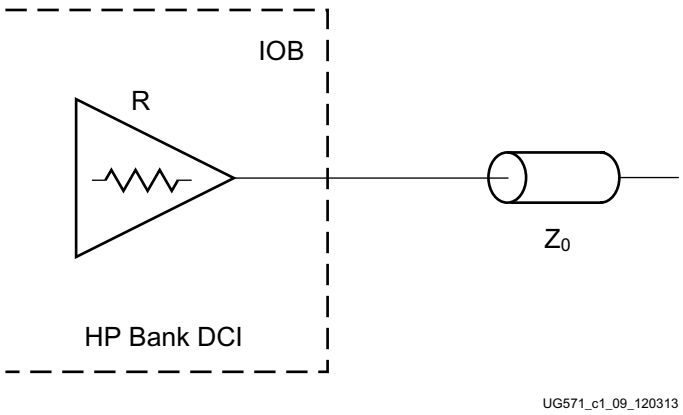

Figure 1-9: **Controlled Impedance Driver**

The DCI input standards supporting the controlled impedance driver are shown in Table 1-2.

Table 1-2: **All DCI I/O Standards Supporting Controlled Impedance Driver**

HSTL_I_DCI	DIFF_HSTL_I_DCI	LVDCI_18	HSUL_12_DCI	DIFF_HSUL_12_DCI	SSTL18_I_DCI	DIFF_SSTL18_I_DCI
HSTL_I_DCI_18	DIFF_HSTL_I_DCI_18	LVDCI_15	POD12_DCI	DIFF_POD12_DCI	SSTL15_DCI	DIFF_SSTL15_DCI
HSTL_I_DCI_12	DIFF_HSTL_I_DCI_12	HSLVDCI_18	POD10_DCI	DIFF_POD10_DCI	SSTL135_DCI	DIFF_SSTL135_DCI
		HSLVDCI_15			SSTL12_DCI	DIFF_SSTL12_DCI

Split-Termination DCI (Thevenin Equivalent Termination to $V_{CCO}/2$)

Some I/O standards (HSTL and SSTL) require an input termination resistance (R) to a V_{TT} voltage of $V_{CCO}/2$ (see Figure 1-10).

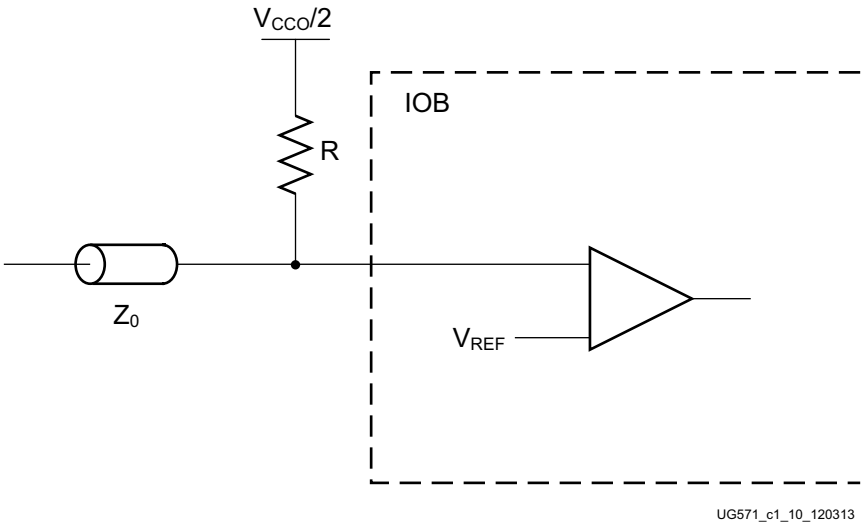

Figure 1-10: **Input Termination to $V_{CCO}/2$ without DCI (where R = Z_0)**

Split-termination DCI creates a Thevenin equivalent circuit using two resistors of twice the resistance value (2R). One terminates to V_{CCO}, the other to GND. Split-termination DCI provides an equivalent termination to $V_{CCO}/2$ using this method. The 2R termination resistance is set by programming the ODT attribute. The resistors to V_{CCO} and GND are equal to twice the value set by ODT. For example, to achieve the Thevenin equivalent parallel-termination circuit of approximately 50Ω to $V_{CCO}/2$, a 240Ω external precision resistor is required at the VRP pin and ODT is set to RTT_48. Possible values for ODT for split-termination DCI are RTT_40, RTT_48, or RTT_60.

The DCI input standards supporting split termination are shown in Table 1-3.

Table 1-3: **All DCI I/O Standards Supporting Split-Termination DCI**

HSTL_I_DCI	DIFF_HSTL_I_DCI	SSTL18_I_DCI	DIFF_SSTL18_I_DCI
HSTL_I_DCI_18	DIFF_HSTL_I_DCI_18	SSTL15_DCI	DIFF_SSTL15_DCI
HSTL_I_DCI_12	DIFF_HSTL_I_DCI_12	SSTL135_DCI	DIFF_SSTL135_DCI
		SSTL12_DCI	DIFF_SSTL12_DCI

Figure 1-11 illustrates split-termination DCI.

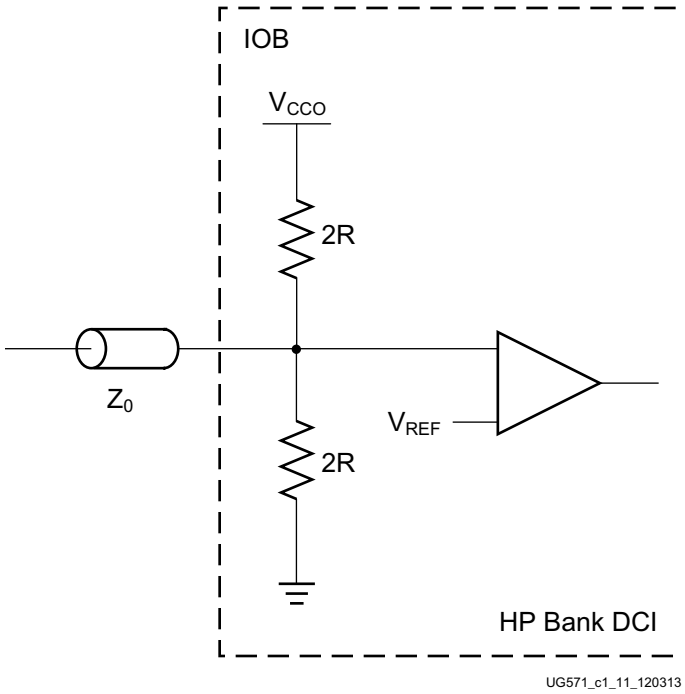

Figure 1-11: **Input Termination to V_{CCO}/2 Using Split-Termination DCI (where R = Z_0)**

Single-Termination DCI

Some I/O standards (POD10, POD12, HSUL_12, and DIFF_HSUL_12) require an input termination resistance (R) to a V_{TT} voltage of V_{CCO} (see Figure 1-12).

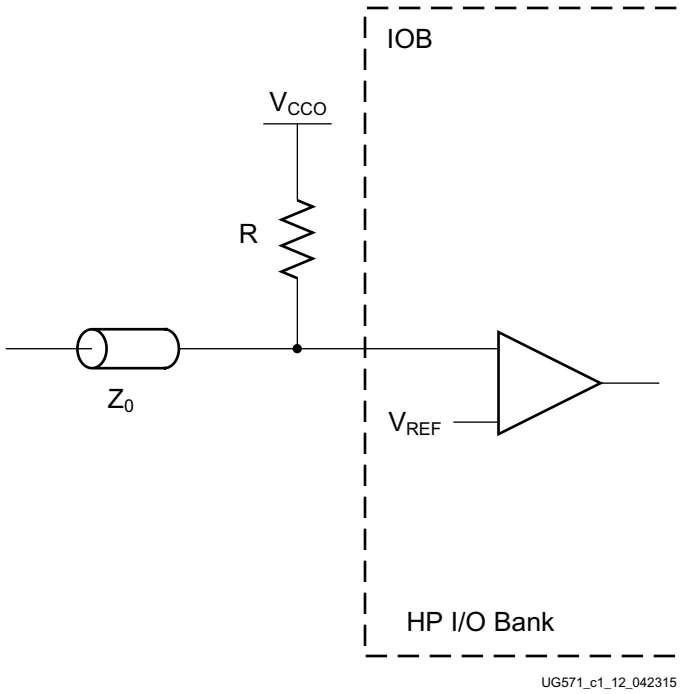

Figure 1-12: **Input termination to V_{CCO} without DCI (where R = Z_0)**

The DCI input standards supporting single termination are shown in Table 1-4.

Table 1-4: **All DCI I/O Standards Supporting Single-Termination DCI**

POD12_DCI	DIFF_POD12_DCI	HSUL_12_DCI
POD10_DCI	DIFF_POD10_DCI	DIFF_HSUL_12_DCI

Single-termination DCI creates a termination to V_{CCO} internally as shown in Figure 1-13. Value of the termination resistor is determined by the ODT attribute. Possible values for ODT:

- POD standards only: RTT_40, RTT_48, and RTT_60
- HSUL_12_DCI and DIFF_HSUL_12_DCI only: RTT_120 and RTT_240
- RTT_NONE

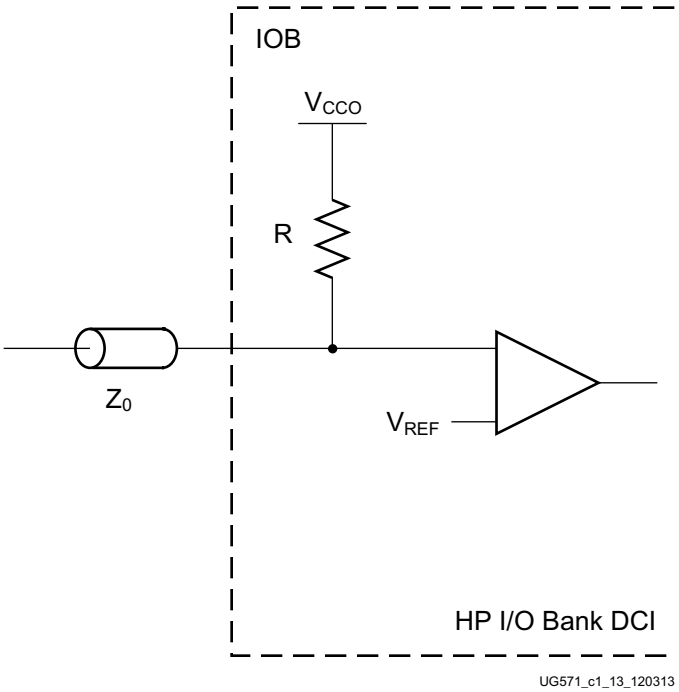

Figure 1-13: **Input termination to V_{CCO} using Single-Termination DCI (where R = Z_0)**

For example, to achieve single termination of approximately 50Ω to V_{CCO} for the POD12_DCI standard, a 240Ω external precision resistor is required at the VRP pin, ODT must be set to the value RTT_48.

VRP External Resistance Design Migration Guidelines

Previous Xilinx FPGA families featuring DCI used a slightly different circuit for calibrating the controlled impedance driver and split-termination impedance from the external reference resistors placed on the VRN and VRP pins. In Xilinx 7 series FPGAs, DCI calibrated each leg of the split-termination circuit to be directly equal to the external resistor values. For example, a 7 series device with a target parallel termination of 50Ω to $V_{CCO}/2$ requires 100Ω external resistors on the VRN and VRP pins.

In UltraScale devices, irrespective of the DCI termination value requirement, the external resistor on the VRP pin is required to be 240Ω. Instead of two resistors, only one resistor is

required at an UltraScale device VRP pin. The exact value of the split-termination or single-termination resistors are determined by the user-controllable ODT attribute.

Possible ODT values for split-termination DCI standards (HSTL and SSTL) are RTT_40, RTT_48, or RTT_60.

IMPORTANT: *The ODT value represents the desired Thevenin resistance to $V_{CCO}/2$ for split-termination DCI standards.*

Possible ODT values for single-termination POD standards are RTT_40, RTT_48, or RTT_60. Possible ODT values for single-termination HSUL standards are RTT_120, RTT_240, or RTT_NONE.

IMPORTANT: *The ODT value represents the desired resistance to V_{CCO} for single-termination DCI standards.*

The termination value for the controlled impedance driver is determined by the DCI state machine when a DCI standard with a controlled impedance driver is chosen, using OUTPUT_IMPEDANCE attribute values. Possible values for OUTPUT_IMPEDANCE attributes are RDRV_40_40, RDRV_48_48, RDRV_60_60, and RDRV_NONE_NONE.

T_DCI Design Migration Guidelines

The Xilinx 7 series architecture supported T_DCI standards for bidirectional I/O configurations with 3-state support for internal input split-termination. Those T_DCI standards are not supported in UltraScale devices. However, many of the UltraScale architecture DCI standards are capable of supporting similar bidirectional configurations. Table 1-5 lists the T_DCI standards that are transparently ported or migrated to an equivalent UltraScale architecture standard when designing with the Vivado® Design Suite.

Table 1-5: **T_DCI I/O Standards for Migration between Xilinx Device Architectures**

7 Series Architecture I/O Standard	UltraScale Architecture Equivalent I/O Standard
DIFF_SSTL15_T_DCI	DIFF_SSTL15_DCI
DIFF_SSTL135_T_DCI	DIFF_SSTL135_DCI
DIFF_SSTL12_T_DCI	DIFF_SSTL12_DCI
SSTL15_T_DCI	SSTL15_DCI
SSTL135_T_DCI	SSTL135_DCI
SSTL12_T_DCI	SSTL12_DCI

DCI I/O Standard Support

DCI supports the standards shown in Table 1-6.

Table 1-6: **All Supported DCI I/O Standards**

LVDCI_18	HSTL_I_DCI	DIFF_HSTL_I_DCI	SSTL18_I_DCI	DIFF_SSTL18_I_DCI
LVDCI_15	HSTL_I_DCI_18	DIFF_HSTL_I_DCI_18	SSTL15_DCI	DIFF_SSTL15_DCI
HSLVDCI_18	HSTL_I_DCI_12	DIFF_HSTL_I_DCI_12	SSTL135_DCI	DIFF_SSTL135_DCI
HSLVDCI_15			SSTL12_DCI	DIFF_SSTL12_DCI
			HSUL_12_DCI	DIFF_HSUL_12_DCI
			POD12_DCI	DIFF_POD12_DCI
			POD10_DCI	DIFF_POD10_DCI

To correctly use DCI:

1. V_{CCO} pins must be connected to the appropriate V_{CCO} voltage based on the I/O standards in that I/O bank.
2. Correct DCI I/O buffers must be used in the Vivado Design Suite either by using I/O standard attributes or instantiations in the HDL code.
3. DCI standards require connecting an external reference resistor to the multipurpose VRP pin. When this is required, that multipurpose pin cannot be used as a general-purpose I/O in the I/O bank using DCI or in the master I/O bank when cascading DCI. See the pinout tables for the specific pin locations. The VRP pin must be pulled to GND by a reference resistor. An exception to this requirement comes when cascading DCI in slave I/O banks because the VRP pin can be used as general-purpose I/O.
4. The value of the external reference resistor is fixed at 240Ω, terminated to GND.
5. Follow the DCI I/O banking rules:
   a. V_{REF} must be compatible for all of the inputs in the same I/O bank or in a group of I/O banks when using DCI cascade.
   b. V_{CCO} must be compatible for all of the inputs and outputs in the same I/O bank.
   c. Impedances are no longer constrained by R_{VRP} (240Ω). The DCI state machine calculates the appropriate scaling for controlled impedance drivers, and split and single-termination configurations using OUTPUT_IMPEDANCE and ODT attribute values.

Uncalibrated Input Termination in I/O Banks

The HR I/O and HP I/O banks have an optional uncalibrated input on-chip split-termination feature for HSTL and SSTL standards and a single-termination feature for POD and HSUL standards that are similar to the DCI feature. This option creates a Thevenin equivalent circuit using two internal resistors of twice the target resistance value (2R where R = Z_0) for HSTL and SSTL standards. One resistor terminates to V_{CCO} and the other to GND, providing a Thevenin equivalent termination circuit of half the resistor value to the mid-point $V_{CCO}/2$ for HSTL and SSTL standards. A single resistor terminates to V_{CCO} for POD and HSUL standards.

The termination is present constantly on inputs, and on bidirectional pins whenever the output buffer is 3-stated except when DCITERMDISABLE (in HP I/O banks) or INTERMDISABLE (in HR I/O banks) are asserted. However, an important difference between this uncalibrated option and DCI is that instead of calibrating to an external reference resistor on the VRP pin when using DCI, the uncalibrated input termination feature invokes internal resistors determined by the ODT attribute that have no calibration routine to compensate for temperature, process, or voltage variations.

- Possible ODT values for split-termination standards (HSTL and SSTL) are RTT_40, RTT_48, RTT_60, or RTT_NONE.
- Possible values for ODT for single-termination POD standards are RTT_40, RTT_48, RTT_60, or RTT_NONE.
- Possible values for ODT for single-termination HSUL standards are RTT_120, RTT_240, or RTT_NONE.

The main difference in how DCI or uncalibrated termination is invoked in a design is whether or not a DCI I/O standard is chosen. In both DCI and uncalibrated I/O standards, the values of the termination resistors are determined by the ODT attribute.

Table 1-7 shows a list of I/O standards that support the uncalibrated termination in both the HR and HP I/O banks.

Table 1-7: **I/O Standards that Support Uncalibrated Termination**

HSTL_I	DIFF_HSTL_I	SSTL18_I	DIFF_SSTL18_I	POD12	DIFF_POD12
HSTL_II	DIFF_HSTL_II	SSTL18_II	DIFF_SSTL18_II	POD10	DIFF_POD10
HSTL_I_18	DIFF_HSTL_I_18	SSTL15_R	DIFF_SSTL15_R	HSUL_12	DIFF_HSUL_12
HSTL_II_18	DIFF_HSTL_II_18	SSTL15	DIFF_SSTL15		
		SSTL135_R	DIFF_SSTL135_R		
		SSTL135	DIFF_SSTL135		
		SSTL12	DIFF_SSTL12		

Uncalibrated Source Termination in HP I/O banks

HP I/O banks have an optional uncalibrated source termination feature for SSTL, HSTL, POD, and HSUL standards that is similar to DCI. This feature provides an option of 40Ω, 48Ω, or a 60Ω driver for the supported standards to match the characteristic impedance of the driven line.

An important difference between this uncalibrated option and DCI is that instead of calibrating to an external reference resistor on the VRP pin when using DCI, the uncalibrated source termination feature invokes internal resistors determined by the OUTPUT_IMPEDANCE attribute where no calibration routine is available to compensate for temperature, process, or voltage variations.

IMPORTANT: *This feature is only available in HP I/O banks.*

The allowed values for OUTPUT_IMPEDANCE are RDRV_40_40, RDRV_48_48, or RDRV_60_60.

The main difference in how DCI or uncalibrated termination is invoked in a design is determined when choosing to use either a DCI I/O standard or an uncalibrated one. In both DCI and uncalibrated I/O standards, source termination value is determined by the attribute OUTPUT_IMPEDANCE.

Table 1-8 shows a list of I/O standards that support uncalibrated source termination in HP I/O banks.

Table 1-8: **I/O Standards that Support Uncalibrated Source Termination in HP I/O Banks**

HSTL_I	DIFF_HSTL_I	SSTL18_I	DIFF_SSTL18_I	POD12	DIFF_POD12
HSTL_I_18	DIFF_HSTL_I_18	SSTL15	DIFF_SSTL15	POD10	DIFF_POD10
HSTL_I_12	DIFF_HSTL_I_12	SSTL135	DIFF_SSTL135	HSUL_12	DIFF_HSUL_12
		SSTL12	DIFF_SSTL12		

Receiver Offset Control in HP I/O Banks

In HP I/O banks, for a subset of I/O standards, the UltraScale architecture provides the option of canceling the inherent offset of the input buffers that occurs due to process variations (up to ±35 mV). This feature can be accessed through IBUFE3, IBUFDSE3, IOBUFE3, and IOBUFDSE3 primitives as shown in Figure 1-14 and Figure 1-15. Offset calibration requires building control logic into your interconnect logic design.

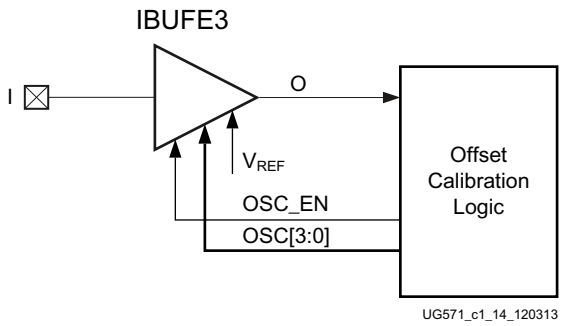

Figure 1-14: **Offset Calibration Connections for Single-Ended I/O Standards**

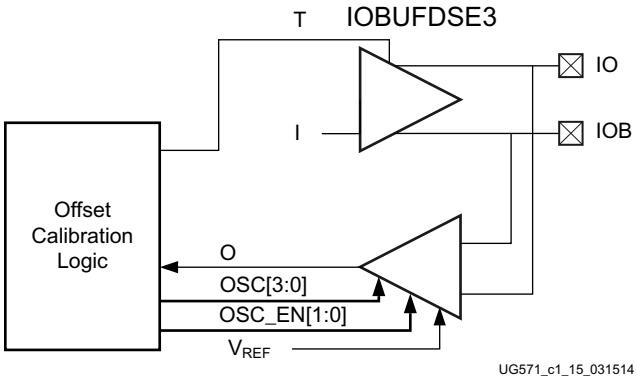

Figure 1-15: **Offset Calibration Connections for Differential I/O Standards**

1. The offset cancellation feature is activated for the supported I/O standards when:
   a. Offset control attribute OFFSET_CNTRL is set to FABRIC.
   b. OSC_EN port is set to `1'b1` (single-ended I/O standards) or `2'b11` (for differential I/O standards).

IMPORTANT: *The value of `2'b10` or `2'b01` is illegal when using OSC_EN for differential I/O standards.*

2. Once the offset cancellation feature is activated, the input to the buffer is pulled-up to V_{REF} (in differential I/Os, both legs are pulled-up to V_{REF}). Based on the inherent offset of the buffer, the output (O) is either a logic 1 or 0. A logic 1 suggests a positive offset. A logic 0 suggests a negative offset. In simulation, this hardware behavior can be

mimicked by setting the simulation-only attribute SIM_INPUT_BUFFER_OFFSET to a negative or positive value from –50 mV to +50 mV. This simulation-only attribute is supported with IBUFE3, IBUFDSE3, IOBUFE3, and IOBUFDSE3 primitives.

3. Based on the value of O, the FABRIC calibration logic should sweep OSC[3:0] in the positive or negative direction until O is seen to flip. The value where O flips is the required offset to cancel the inherent offset of the buffer. Table 1-9 shows the approximate amount of offset cancellation provided by each setting of OSC.

Table 1-9: **Approximate Amount of Offset Cancellation for Each Setting of OSC**

OSC[3:0]	Estimated Offset Cancellation (mV)	OSC[3:0]	Estimated Offset Cancellation (mV)
0000	0	1000	0
0001	–5	1001	5
0010	–10	1010	10
0011	–15	1011	15
0100	–20	1100	20
0101	–25	1101	25
0110	–30	1110	30
0111	–35	1111	35

For example, if the buffer input offset is 15 mV, setting OSC[3:0] = 1011 cancels the offset. If the buffer input offset is –10 mV, setting OSC[3:0] = 0010 cancels the offset.

4. If O does not flip, even at the maximum possible offset (–35mV or 35mV), OSC should be set to the maximum –35mV (0111) if O stays at a logic 1 throughout, or +35mV (1111) if O stays at a logic 0 throughout and continue to step 5.
5. Once the required offset is determined, OSC_EN should be turned off by setting it to 1'b0 (single ended I/O standards) or 2'b00 (differential I/O standards) and normal operation can resume.

RECOMMENDED: *Offset calibration should not be attempted on inputs with external bias or termination.*

IMPORTANT: *OSC[3:0] is a shared bus among all the I/Os within a half bank (26 consecutive I/Os in the top half or bottom half of a bank).*

The I/O standards that support receiver offset control are shown in Table 1-10.

Table 1-10: **I/O Standards Supporting Receiver Offset Control**

POD12	DIFF_POD12
POD12_DCI	DIFF_POD12_DCI

Receiver V_{REF} Scan in HP I/O Banks

An optional V_{REF} scan feature in HP I/O banks helps to fine tune the internal V_{REF} of input buffers to maximize the performance for a subset of I/O standards. This feature can be accessed through the IBUFE3 and IOBUFE3 primitives in conjunction with the HPIO_VREF primitive as shown in Figure 1-16. V_{REF} scan requires building control logic into your interconnect logic design.

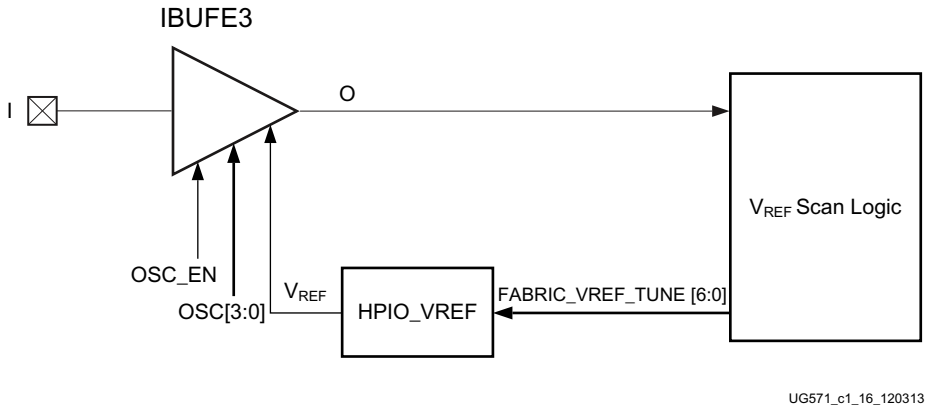

Figure 1-16: **Connection from the Interconnect Logic to access the V_{REF} Scan Feature**

Internal V_{REF} tuned using the V_{REF} scan feature controls the V_{REF} of 13 consecutive I/Os (1 byte group) within a bank as shown in Figure 1-17. There are four byte groups within a bank. Four different variations of a given V_{REF} are possible within a bank (for four byte groups in each bank). However, to use this feature, the central V_{REF} of the bank needs to be set using the INTERNAL_VREF attribute (See Internal V_{REF}). Inputs with I/O standards of different V_{REF} specifications cannot be placed within the same bank. Tuned V_{REF} connection (V_{REF} output of HPIO_VREF primitive) cannot traverse byte group boundaries.

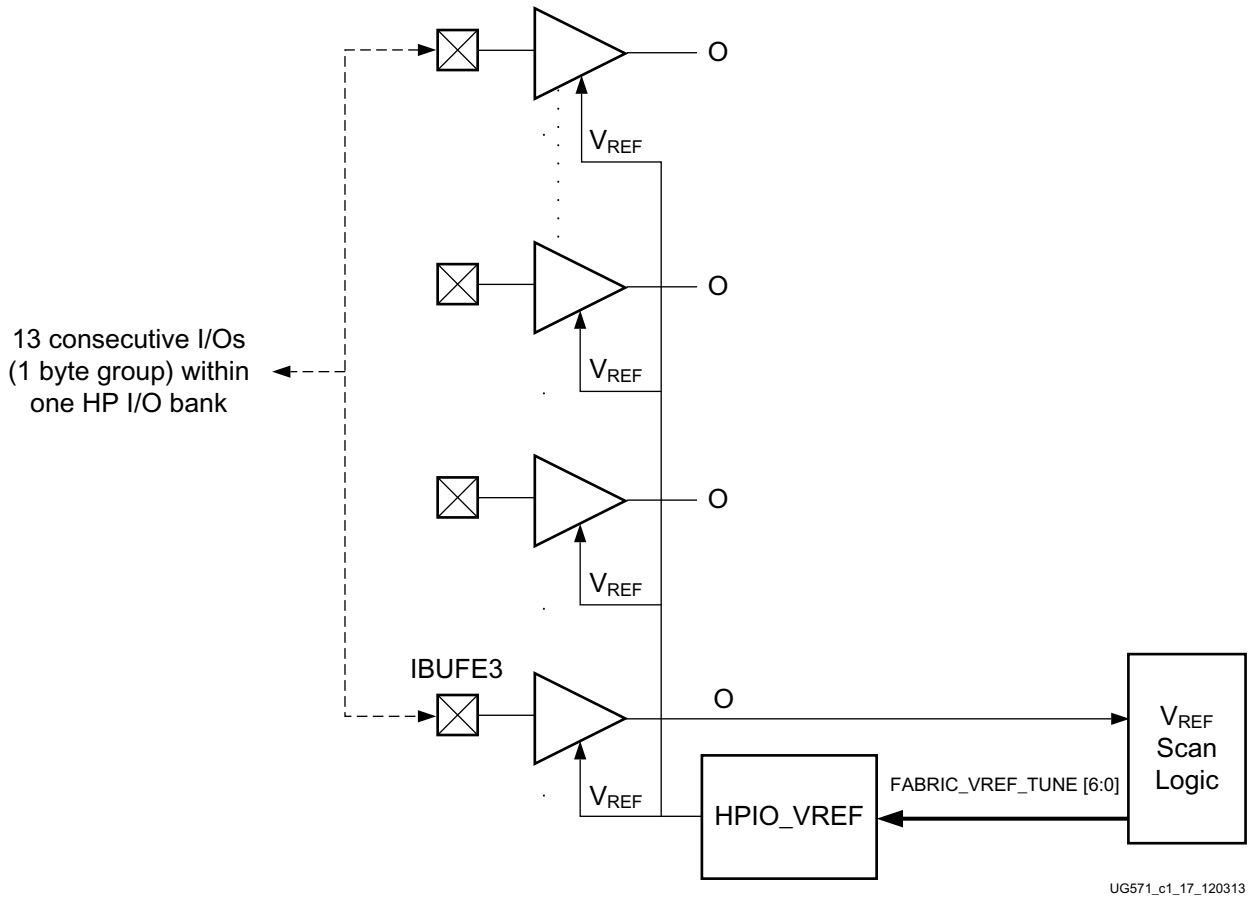

Figure 1-17: **V_{REF} Scan Connection per Byte Group within a Bank**

Internal V_{REF} (INTERNAL_VREF and V_{REF} scan) cannot be combined with external V_{REF} usage within a bank.

SelectIO Primitives

The Vivado Design Suite library includes an extensive list of primitives supporting many I/O standards available in the I/O primitives. These generic primitives can each support most of the available single-ended I/O standards.

- IBUF (input buffer)
- IBUF_ANALOG (input buffer specific to system monitor inputs). The IBUF_ANALOG is used by the Vivado Design Suite tools to route analog signals to the SYSMONE1 primitive. It is not a physical buffer and is purely a software construct that should be viewed as a physical pass through.
- IBUF_IBUFDISABLE (input buffer with buffer disable control)

- IBUF_INTERMDISABLE (input buffer with buffer disable and on-die input termination disable controls (HR I/O banks only))
- IBUFE3 (input buffer with offset calibration and V_{REF} tuning, along with buffer disable control (HP I/O banks only))
- IOBUF (bidirectional buffer)
- OBUF (output buffer)
- OBUFT (3-state output buffer)
- IOBUF_DCIEN (bidirectional buffer with input buffer disable and on-die input termination disable control (HP I/O banks only))
- IOBUF_INTERMDISABLE (bidirectional buffer with input buffer disable and on-die input termination disable control (HR I/O banks only))
- IOBUFE3 (bidirectional buffer with offset calibration and V_{REF} tuning, along with input buffer disable and on-die input termination enable control (HP I/O banks only))

These generic primitives can each support most of the available differential I/O standards:

- IBUFDS (differential input buffer)
- IBUFDS_DIFF_OUT (differential input buffer with complementary outputs)
- IBUFDS_DIFF_OUT_IBUFDISABLE (differential input buffer with complementary outputs and buffer disable)
- IBUFDS_DIFF_OUT_INTERMDISABLE (differential input buffer with complementary outputs, input buffer disable and on-die input termination disable control (HR I/O banks only))
- IBUFDS_IBUFDISABLE (differential input buffer with buffer disable control)
- IBUFDS_INTERMDISABLE (differential input buffer with input buffer disable and on-die input termination disable control (HR I/O banks only))
- IBUFDSE3 (differential input buffer with offset calibration along with buffer disable control (HP I/O banks only))
- IOBUFDS (differential bidirectional buffer)
- IOBUFDS_DCIEN (differential bidirectional buffer with on-die input termination disable control and input buffer disable (HP I/O banks only))
- IOBUFDS_DIFF_OUT (differential bidirectional buffer with complementary outputs from the input buffer)
- IOBUFDS_DIFF_OUT_DCIEN (differential bidirectional buffer with complementary outputs from the input buffer with on-die input termination disable controls and input buffer disable controls (HP I/O banks only))

- IOBUFDS_INTERMDISABLE (bidirectional buffer with on-die input termination disable control and input buffer disable (HR I/O banks only))
- IOBUFDS_DIFF_OUT_INTERMDISABLE (bidirectional buffer with complementary outputs from the input buffer with on-die input termination disable control and input buffer disable (HR I/O banks only))
- IOBUFDSE3 (differential bidirectional buffer with offset calibration along with input buffer disable and on-die input termination enable control (HP I/O banks only))
- OBUFDS (differential output buffer)
- OBUFTDS (differential 3-state output buffer)
- HPIO_VREF (V_{REF} scan feature (HP I/O banks only))

More information including instantiation techniques and available attributes for these and all other design primitives is available in the *UltraScale Architecture Libraries Guide* (UG974) [Ref 6].

IBUF

Signals used as inputs must use an input buffer (IBUF). The generic IBUF primitive is shown in Figure 1-18.

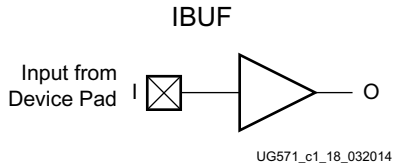

Figure 1-18: **Input Buffer Primitive (IBUF)**

IBUF_IBUFDISABLE

The IBUF_IBUFDISABLE primitive shown in Figure 1-19 is an input buffer with a disable port that can be used as an additional power saving feature for periods when the input is not used.

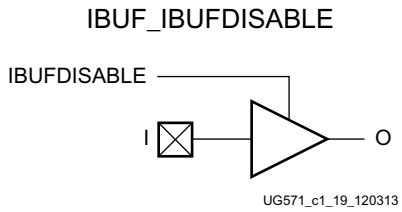

Figure 1-19: **Input Buffer With Input Buffer Disable (IBUF_IBUFDISABLE)**

The IBUF_IBUFDISABLE primitive can disable the input buffer and force the O output to the internal logic to a logic-Low when the IBUFDISABLE signal is asserted High. The USE_IBUFDISABLE attribute must be set to TRUE and SIM_DEVICE to ULTRASCALE for this primitive to have the expected behavior specific to the UltraScale architecture. This feature can be used to reduce power at times when the I/O is idle. Input buffers that use the V_{REF} power rail (such as SSTL and HSTL) benefit the most from the IBUFDISABLE signal being set to a logic-High because they tend to have higher static power consumption than the non-VREF standards such as LVCMOS and LVTTL.

IBUF_INTERMDISABLE

The IBUF_INTERMDISABLE primitive shown in Figure 1-20 is available in the HR I/O banks and is similar to the IBUF_IBUFDISABLE primitive in that it has a IBUFDISABLE port that can be used to disable the input buffer during periods that the buffer is not being used. The USE_IBUFDISABLE attribute must be set to TRUE and SIM_DEVICE to ULTRASCALE for this primitive to have the expected behavior specific to the UltraScale architecture. The IBUF_INTERMDISABLE primitive also has an INTERMDISABLE port that can be used to disable the optional on-die receiver termination feature. See Uncalibrated Input Termination in I/O Banks for more details about this feature.

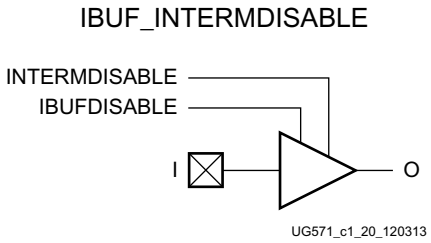

Figure 1-20: **Input Buffer With Input Buffer Disable and On-die Input Termination Disable (IBUF_INTERMDISABLE)**

The IBUF_INTERMDISABLE primitive can disable the input buffer and force the O output to the internal logic to a logic-Low when the IBUFDISABLE signal is asserted High. The IBUF_INTERMDISABLE primitive further allows the termination legs to be disabled whenever the INTERMDISABLE signal is asserted High. These features can be combined to reduce power whenever the input is idle. Input buffers that use the V_{REF} power rail (such as SSTL and HSTL) benefit the most from the IBUFDISABLE signal being set to a logic-High because they tend to have higher static power consumption than the non-V_{REF} standards such as LVCMOS and LVTTL.

IBUFE3

The input buffer (IBUFE3) primitive (shown in Figure 1-21) is only supported in HP I/O banks. This UltraScale architecture specific primitive has functions similar to the IBUF with added controls for offset calibration and V_{REF} tuning, along with input buffer disable (IBUFDISABLE). The offset calibration feature is accessed using the OSC_EN and OSC[3:0] ports. The V_{REF} scan feature is accessed using the HPIO_VREF primitive in conjunction with IBUFE3.

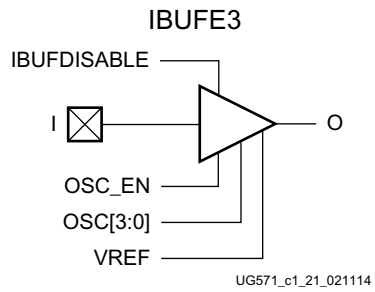

Figure 1-21: **IBUFE3 Primitive—Input Buffer with Offset Calibration and V_{REF} Tuning (HP I/O Banks Only)**

IBUFDS

The usage and rules corresponding to the differential primitives are similar to the single-ended SelectIO primitives. Differential SelectIO primitives have two pins to and from the device pads to show the P and N channel pins in a differential pair. N channel pins have a B suffix.

Figure 1-22 shows the differential input buffer primitive.

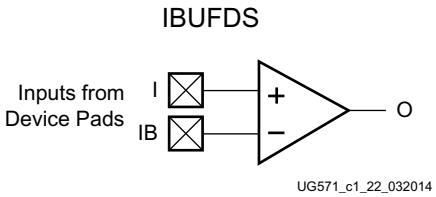

Figure 1-22: **Differential Input Buffer Primitive (IBUFDS)**

IBUFDS_DIFF_OUT

Figure 1-23 shows the differential input buffer primitive with complementary outputs (O and OB).

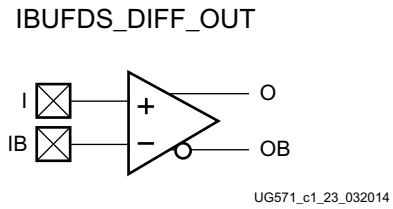

Figure 1-23: **Differential Input Buffer Primitive With Complementary Outputs (IBUFDS_DIFF_OUT)**

IBUFDS_DIFF_OUT_IBUFDISABLE

The IBUFDS_DIFF_OUT_IBUFDISABLE primitive shown in Figure 1-24 is a differential input buffer with complementary differential outputs. The USE_IBUFDISABLE attribute must be set to TRUE and the SIM_DEVICE to ULTRASCALE for this primitive to have the expected behavior that is specific to the UltraScale architecture.

TIP: *The IBUFDISABLE feature is not supported with this primitive in the UltraScale architecture.*

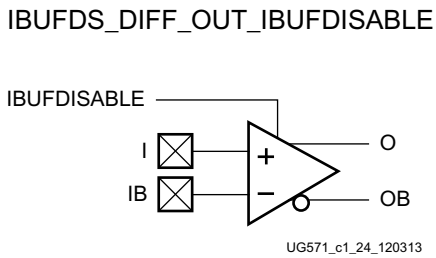

Figure 1-24: **Differential Input Buffer With Complementary Outputs and Input Buffer Disable (IBUFDS_DIFF_OUT_IBUFDISABLE)**

IBUFDS_DIFF_OUT_INTERMDISABLE

The IBUFDS_DIFF_OUT_INTERMDISABLE primitive shown in Figure 1-25 is available in the HR I/O banks. It has complementary differential outputs and an INTERMDISABLE port that can be used to manually disable the optional on-die receiver termination features (uncalibrated). See Uncalibrated Input Termination in I/O Banks for more details. The USE_IBUFDISABLE attribute must be set to TRUE and SIM_DEVICE to ULTRASCALE for this primitive to have the expected behavior that is specific to the UltraScale architecture.

TIP: *The IBUFDISABLE feature is not supported with this primitive in the UltraScale architecture.*

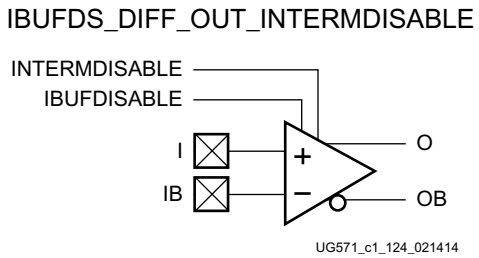

Figure 1-25: **Differential Input Buffer with Complementary Outputs, Input Path Disable, and On-die Input Termination Disable (IBUFDS_DIFF_OUT_INTERMDISABLE)**

If the I/O is using any on-die receiver termination features (uncalibrated), this primitive disables the termination legs whenever the INTERMDISABLE signal is asserted High.

IBUFDS_IBUFDISABLE

The IBUFDS_IBUFDISABLE primitive shown in Figure 1-26 is a differential input buffer with a disable port that can be used as an additional power saving feature for periods when the input is not used.

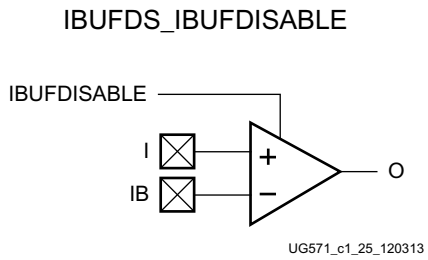

Figure 1-26: **Differential Input Buffer With Input Buffer Disable (IBUFDS_IBUFDISABLE)**

The IBUFDS_IBUFDISABLE primitive can disable the input buffer and force the O output to the internal logic to a logic-Low when the IBUFDISABLE signal is asserted High. The USE_IBUFDISABLE attribute must be set to TRUE and SIM_DEVICE to ULTRASCALE for this

primitive to have the expected behavior that is specific to the UltraScale architecture. This feature can be used to reduce power whenever the I/O is idle.

IBUFDS_INTERMDISABLE

The IBUFDS_INTERMDISABLE primitive (shown in Figure 1-27), available in the HR I/O banks, is similar to the IBUFDS_IBUFDISABLE primitive because it has a IBUFDISABLE port to disable the input buffer when not in use. The IBUFDS_INTERMDISABLE primitive also has an INTERMDISABLE port to use to disable the optional on-die receiver termination feature. See Uncalibrated Input Termination in I/O Banks for more details.

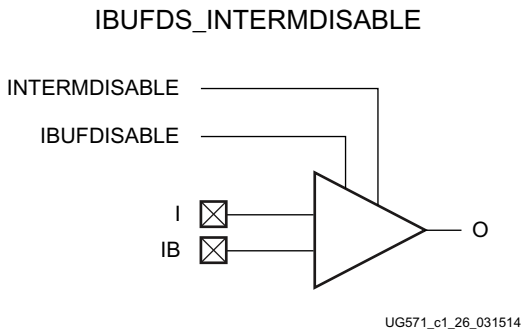

Figure 1-27: **Differential Input Buffer With Input Buffer Disable and On-die Input Termination Disable (IBUFDS_INTERMDISABLE)**

The IBUFDS_INTERMDISABLE primitive can disable the input buffer and force the O output to a logic-Low when the IBUFDISABLE signal is asserted High. The USE_IBUFDISABLE attribute must be set to TRUE and SIM_DEVICE to ULTRASCALE for this primitive to have the expected behavior that is specific to the UltraScale architecture. If the I/O is using the optional on-die receiver termination feature, this primitive disables the termination legs whenever the INTERMDISABLE signal is asserted High. Both these features can be combined to reduce power whenever the input is idle.

IBUFDSE3

The differential input buffer (IBUFDSE3) primitive is only supported in HP I/O banks. This UltraScale architecture specific primitive has functions similar to the IBUFDS along with controls for offset calibration and input buffer disable (IBUFDISABLE). The offset calibration feature is accessed using the OSC_EN and OSC[3:0] ports. The V_{REF} scan feature is not supported with this primitive.

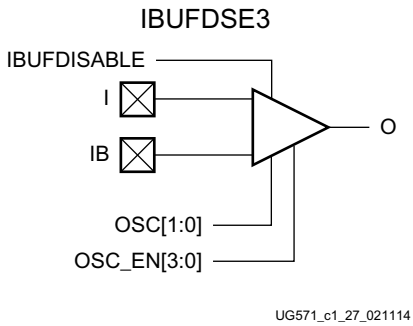

Figure 1-28: **IBUFDSE3 Primitive—Differential Input Buffer with Offset Calibration (HP I/O Banks Only)**

IOBUF

The IOBUF primitive is needed when bidirectional signals require both an input buffer and a 3-state output buffer with an active-High 3-state T pin. Figure 1-29 shows a generic IOBUF. A logic-High on the T pin disables the output buffer. When the output buffer is 3-stated (T = High), the input buffer and any on-die receiver termination (uncalibrated or DCI) are ON. When the output buffer is not 3-stated (T = Low), any on-die receiver termination (uncalibrated or DCI) is disabled.

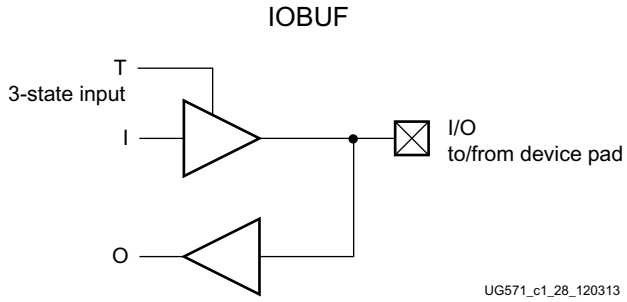

Figure 1-29: **Input/Output Buffer Primitive (IOBUF)**

IOBUF_DCIEN

The IOBUF_DCIEN primitive shown in Figure 1-30 is available in the HP I/O banks. It has an IBUFDISABLE port that can be used to disable the input buffer during periods that the buffer is not being used. The IOBUF_DCIEN primitive also has a DCITERMDISABLE port that can be used to manually disable the optional on-die receiver termination features (uncalibrated and DCI). See the DCI—Only available in the HP I/O Banks and Uncalibrated Input Termination in I/O Banks sections for more details.

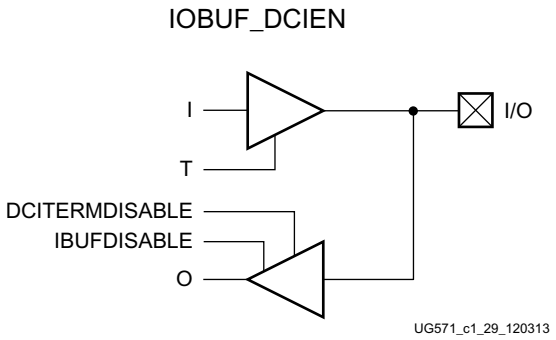

Figure 1-30: **Input/Output Buffer DCI Enable Primitive (IOBUF_DCIEN)**

The IOBUF_DCIEN primitive can disable the input buffer and force the O output to the internal logic to a logic-Low when the IBUFDISABLE signal is asserted High and output buffer is 3-stated (T = High). If the I/O is using any on-die receiver termination features (uncalibrated and DCI), this primitive disables the termination legs whenever the DCITERMDISABLE signal is asserted High and the output buffer is 3-stated (T = High). When the output buffer is 3-stated (T = High), the input buffer and any on-die receiver termination (uncalibrated or DCI) are controlled by IBUFDISABLE and DCITERMDISABLE, respectively. The USE_IBUFDISABLE attribute must be set to TRUE and SIM_DEVICE to ULTRASCALE for this primitive to have the expected behavior that is specific to the UltraScale architecture. When the output buffer is not 3-stated (T = Low), the input buffer and any on-die receiver termination (uncalibrated or DCI) are disabled and the O output (to the internal logic) is forced to a logic-Low. These features can be combined to reduce power whenever the input is idle for a period of time.

IOBUF_INTERMDISABLE

The IOBUF_INTERMDISABLE primitive shown in Figure 1-31 is available in the HR I/O banks. It has an IBUFDISABLE port that can be used to disable the input buffer during periods that the buffer is not being used. The IOBUF_INTERMDISABLE primitive also has an INTERMDISABLE port that can be used to manually disable the optional on-die receiver termination feature. See Uncalibrated Input Termination in I/O Banks for more details.

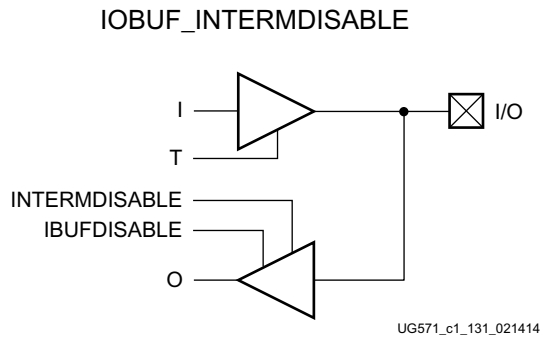

Figure 1-31: **Bidirectional Buffer with Input Path Disable and On-die Input Termination Disable (IOBUF_INTERMDISABLE)**

The IOBUF_INTERMDISABLE primitive can disable the input buffer and force the O output to the internal logic to a logic-Low when the IBUFDISABLE signal is asserted High and the output buffer is 3-stated (T = High). If the I/O is using the on-die receiver termination feature (uncalibrated), this primitive disables the termination legs whenever the INTERMDISABLE signal is asserted High and the output buffer is 3-stated (T = High). When the output buffer is 3-stated (T = High), the input buffer and any on-die receiver termination are controlled by IBUFDISABLE and INTERMDISABLE, respectively. The USE_IBUFDISABLE attribute must be set to TRUE and the SIM_DEVICE set to ULTRASCALE for this primitive to have the expected behavior that is specific to the UltraScale architecture. When the output buffer is not 3-stated (T = Low), the input buffer and any on-die receiver termination are disabled and the O output (to the internal logic) is forced to a logic-Low. These features can be combined to reduce power whenever the input is idle for a period of time.

IOBUFE3

The bidirectional input/output buffer primitive (IOBUFE3) is only supported in HP I/O banks (Figure 1-32). This UltraScale architecture specific primitive has functions similar to the IOBUF along with controls for offset calibration and V_{REF} tuning with input buffer disable (IBUFDISABLE) and on-die input termination control (DCITERMDISABLE) for the input buffer. The offset calibration feature is accessed using the OSC_EN and OSC[3:0] ports. The V_{REF} scan feature is accessed using the HPIO_VREF primitive in conjunction with IOBUFE3.

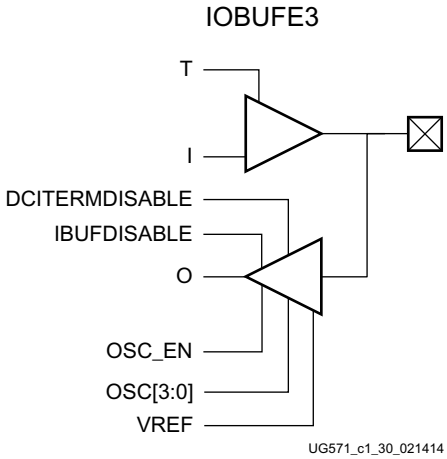

Figure 1-32: **IOBUFE3 Primitive—Bidirectional I/O Buffer with Offset Calibration and V_{REF} Tuning (HP I/O Banks Only)**

IOBUFDS

Figure 1-33 shows the differential input/output buffer primitive. A logic-High on the T pin disables the output buffer. When the output buffer is 3-stated (T = High), the input buffer and any on-die receiver termination (uncalibrated or DCI) are ON. When the output buffer is not 3-stated (T = Low), any on-die receiver termination (uncalibrated or DCI) is disabled.

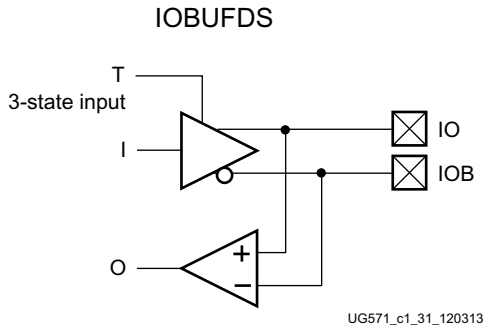

Figure 1-33: **Differential Input/Output Buffer Primitive (IOBUFDS)**

IOBUFDS_DCIEN

The IOBUFDS_DCIEN primitive shown in Figure 1-34 is available in the HP I/O banks. It has an IBUFDISABLE port that can be used to disable the input buffer during periods that the buffer is not being used. The USE_IBUFDISABLE attribute must be set to TRUE and SIM_DEVICE to ULTRASCALE for this primitive to have the expected behavior that is specific to the UltraScale architecture. The IOBUFDS_DCIEN primitive also has a DCITERMDISABLE port that can be used to manually disable the optional on-die receiver termination features (uncalibrated or DCI). See DCI—Only available in the HP I/O Banks and Uncalibrated Input Termination in I/O Banks for more details.

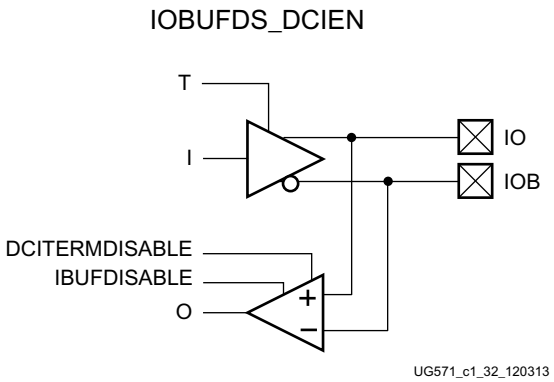

Figure 1-34: **Differential Bidirectional Buffer With Input Buffer Disable and On-die Input Termination Disable (IOBUFDS_DCIEN)**

The IOBUFDS_DCIEN primitive can disable the input buffer and force the O output to the internal logic to a logic-Low when the IBUFDISABLE signal is asserted High and the output buffer is 3-stated (T = High). If the I/O is using an on-die receiver termination feature (uncalibrated or DCI), this primitive disables the termination legs whenever the DCITERMDISABLE signal is asserted High and the output buffer is 3-stated (T = High).

When the output buffer is 3-stated (T = High), the input buffer and any on-die receiver termination (uncalibrated or DCI) are controlled by IBUFDISABLE and DCITERMDISABLE, respectively. When the output buffer is not 3-stated (T = Low), the input buffer and any on-die receiver termination (uncalibrated or DCI) are disabled and force the O output (to the internal logic) to a logic-Low. These features can be combined to reduce power whenever the input is idle for a period of time.

IOBUFDS_DIFF_OUT

Figure 1-35 shows the differential input/output buffer primitive with complementary outputs (O and OB). A logic-High on the T pin disables the output buffers. When the output buffers are 3-stated (T = High), the input buffer and any on-die receiver termination (uncalibrated or DCI) are ON. When the output buffer is not 3-stated (T = Low), any on-die receiver termination (uncalibrated or DCI) is disabled. TM and TS must be connected to the same input from the interconnect logic for this primitive to have the expected behavior that is specific to the UltraScale architecture.

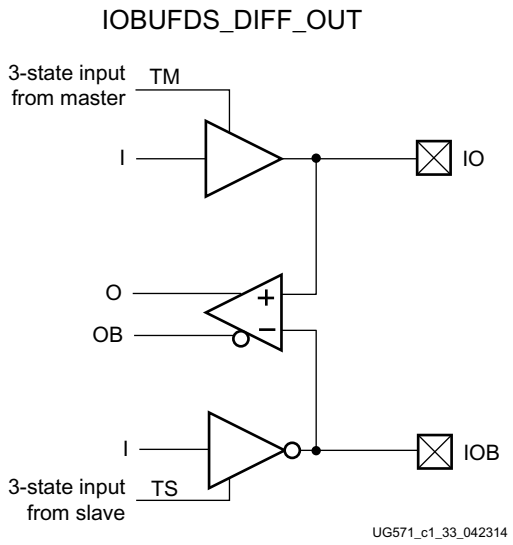

Figure 1-35: **Differential Input/Output Buffer Primitive With Complementary Outputs for the Input Buffer (IOBUFDS_DIFF_OUT)**

IOBUFDS_DIFF_OUT_DCIEN

The IOBUFDS_DIFF_OUT_DCIEN primitive shown in Figure 1-36 is available in the HP I/O banks. It has complementary differential outputs, an IBUFDISABLE port, and a DCITERMDISABLE port that can be used to manually disable the optional DCI on-die receiver termination features (uncalibrated or DCI). See DCI—Only available in the HP I/O Banks and Uncalibrated Input Termination in I/O Banks for more details. The USE_IBUFDISABLE attribute must be set to TRUE and SIM_DEVICE to ULTRASCALE for this primitive to have the expected behavior that is specific to the UltraScale architecture. TM and TS must be connected to the same input from the interconnect logic for this primitive to have the expected behavior that is specific to the UltraScale architecture.

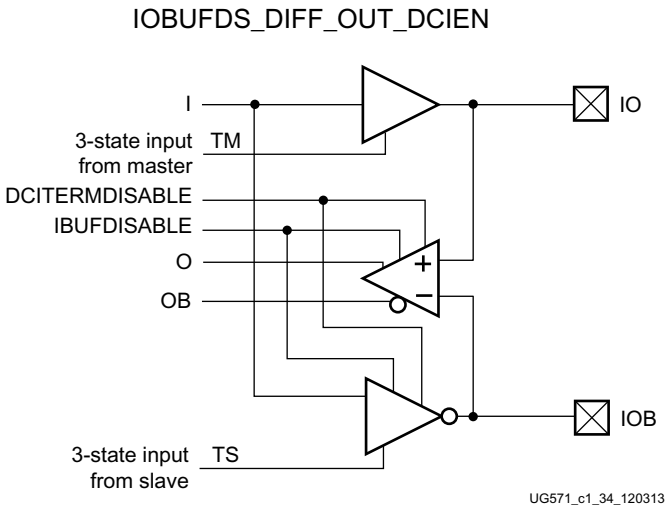

Figure 1-36: **Differential Bidirectional Buffer with Complementary Outputs, Input Path Disable, and On-die Input Termination Disable (IOBUFDS_DIFF_OUT_DCIEN)**

If the I/O is using any on-die receiver termination features (uncalibrated or DCI), this primitive disables the termination legs whenever the DCITERMDISABLE signal is asserted High and the output buffer is 3-stated. When the output buffer is 3-stated (T = High), any on-die receiver termination (uncalibrated or DCI) is controlled by DCITERMDISABLE. When the output buffer is not 3-stated (T = Low), the input buffer and on-die receiver termination (uncalibrated or DCI) are disabled and the O output (to the internal logic) is forced to a logic-Low.

TIP: *The IBUFDISABLE feature is not supported with this primitive in the UltraScale architecture.*

IOBUFDS_INTERMDISABLE

The IOBUFDS_INTERMDISABLE primitive (shown in Figure 1-37) is available in the HR I/O banks. It has an IBUFDISABLE port that can be used to disable the input buffer during periods when the buffer is not being used. The IOBUFDS_INTERMDISABLE primitive also has an INTERMDISABLE port that can be used to disable the optional on-die receiver termination feature. See Uncalibrated Input Termination in I/O Banks for more details on this feature.

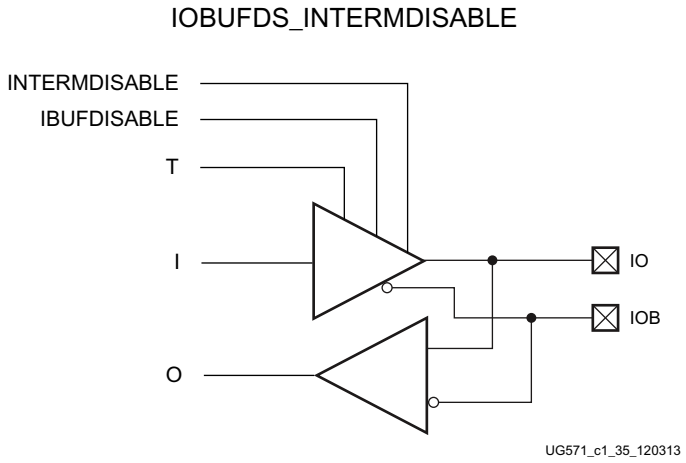

Figure 1-37: **Differential Bidirectional Buffer With Input Buffer Disable and On-die Input Termination Disable (IOBUFDS_INTERMDISABLE)**

The IOBUFDS_INTERMDISABLE primitive can disable the input buffer and force the O output to the internal logic to a logic-Low when the IBUFDISABLE signal is asserted High and the output buffer is 3-stated (T = High). The USE_IBUFDISABLE attribute must be set to TRUE and SIM_DEVICE to ULTRASCALE for this primitive to have the expected behavior that is specific to the UltraScale architecture. If the I/O is using the on-die receiver termination feature, this primitive disables the termination legs whenever the INTERMDISABLE signal is asserted High and the output buffer is 3-stated. When the output buffer is 3-stated (T = High), the input buffer and any on-die receiver termination are controlled by IBUFDISABLE and INTERMFIDISABLE, respectively. When the output buffer is not 3-stated (T = Low), the input buffer and on-die receiver termination are disabled and the O output (to the internal logic) is forced to a logic-Low. These features can be combined to reduce power whenever the input is idle for a period of time.

IOBUFDS_DIFF_OUT_INTERMDISABLE

The IOBUFDS_DIFF_OUT_INTERMDISABLE primitive (shown in Figure 1-38) is available in the HR I/O banks. The IOBUFDS_DIFF_OUT_INTERMDISABLE primitive has an INTERMDISABLE port that can be used to disable the optional on-die receiver termination feature. See Uncalibrated Input Termination in I/O Banks for more details on this feature. TM and TS must be connected to the same input (T) from the interconnect logic for this primitive to have the expected behavior that is specific to the UltraScale architecture.

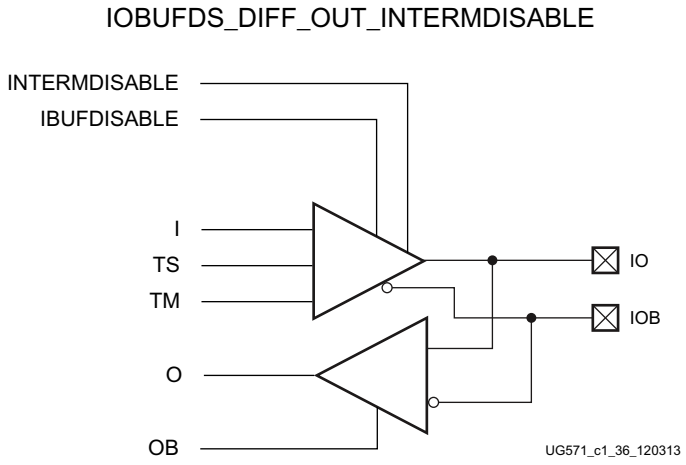

Figure 1-38: **Differential Bidirectional Buffer with Complementary Outputs, Input Buffer Disable, and On-die Input Termination Disable (IOBUFDS_DIFF_OUT_INTERMDISABLE)**

The USE_IBUFDISABLE attribute must be set to TRUE and SIM_DEVICE to ULTRASCALE for the IOBUFDS_DIFF_OUT_INTERMDISABLE primitive to have the expected behavior that is specific to the UltraScale architecture. If the I/O is using the on-die receiver termination features, this primitive disables the termination legs whenever the INTERMDISABLE signal is asserted High and the output buffer is 3-stated. When the output buffer is 3-stated (T = High), any on-die receiver termination is controlled by INTERMDISABLE. When the output buffer is not 3-stated (T = Low), the input buffer and on-die receiver termination are disabled and the O output (to the internal logic) is forced to a logic-Low.

TIP: *The IBUFDISABLE feature is not supported with this primitive in the UltraScale architecture.*

IOBUFDSE3

The differential bidirectional input/output buffer primitive (IOBUFDSE3) is only supported in HP I/O banks. This UltraScale architecture specific primitive has functions similar to the IOBUFDS along with controls for offset calibration with input buffer disable control (IBUFDISABLE) and on-die input termination disable control (DCITERMDISABLE) for the input buffer. The offset calibration feature is accessed using the OSC_EN[1:0] and OSC[3:0] ports. The V_{REF} scan feature is not supported with this primitive.

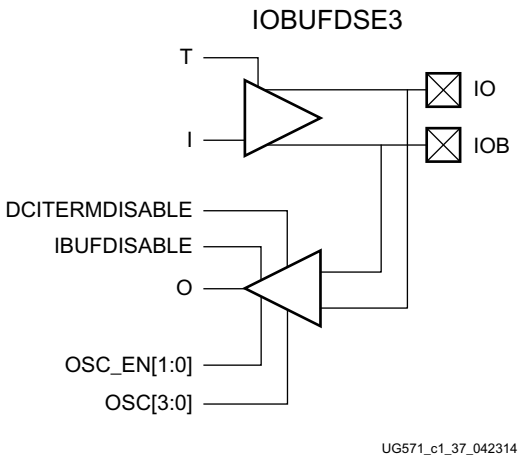

Figure 1-39: **IOBUFDSE3 Primitive—Differential Bidirectional I/O Buffer with Offset Calibration (HP I/O Banks Only)**

OBUF

An output buffer (OBUF) must be used to drive signals from the device to external output pads. A generic OBUF primitive is shown in Figure 1-40.

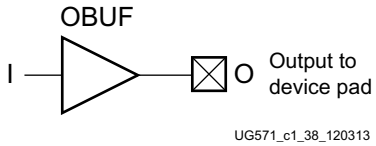

Figure 1-40: **Output Buffer Primitive (OBUF)**

OBUFDS

Figure 1-41 shows the differential output buffer primitive.

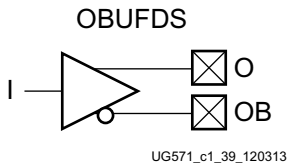

Figure 1-41: **Differential Output Buffer Primitive (OBUFDS)**

OBUFT

The generic 3-state output buffer OBUFT, shown in Figure 1-42, typically implements 3-state outputs or bidirectional I/O.

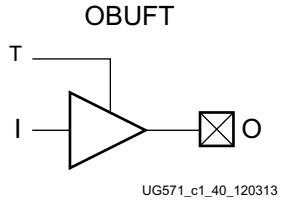

Figure 1-42: **3-State Output Buffer Primitive (OBUFT)**

OBUFTDS

Figure 1-43 shows the differential 3-state output buffer primitive.

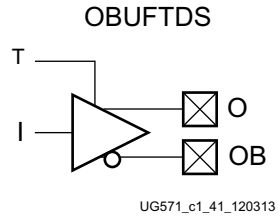

Figure 1-43: **Differential 3-state Output Buffer Primitive (OBUFTDS)**

HPIO_VREF

The HPIO_VREF primitive is only supported in HP I/O banks. This UltraScale architecture specific primitive provides access to the V_{REF} scan feature that is available in HP I/O banks. The V_{REF} scan feature is accessed using the HPIO_VREF primitive in conjunction with either the IBUFE3 or IOBUFE3 primitives.

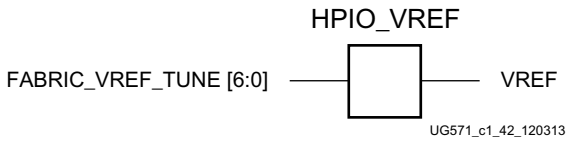

Figure 1-44: **HPIO_VREF Primitive—V_{REF} Scan Feature (HP I/O Banks Only)**

SelectIO Attributes/Constraints

Access to some I/O resource features (for example, location constraints, input delay, output drive strength, and slew rate) is available through the attributes/constraints associated with these features. For more information about implementing these constraints and attributes as well as others, see the *Vivado Design Suite Properties Reference Guide* (UG912) [Ref 7].

DCI_CASCADE Constraint

The DCI_CASCADE constraint identifies a DCI master bank and its corresponding slave banks. See DCI Cascading, page 20 for more information.

The DCI_CASCADE attribute uses the following syntax in the Xilinx Design Constraints (XDC) file:

```
set_property DCI_CASCADE {slave_banks} [get_iobanks master_bank]
```

PACKAGE_PIN Constraint

The PACKAGE_PIN constraint must be used to specify the I/O location of an external port identifier (A8, M5, or AM6). These values are device and package size dependent.

The PACKAGE_PIN attribute uses the following syntax in the XDC file:

```
set_property PACKAGE_PIN pin_name [get_ports port_name]
```

IOSTANDARD Attribute

The IOSTANDARD attribute is available to choose the values for an I/O standard for all I/O buffers. The supported I/O standards are listed in the specific UltraScale device data sheet [Ref 1]; however, Table 1-72 lists the IOSTANDARD support by I/O bank type (HR, HP, or both). The IOSTANDARD attribute uses the following syntax in the XDC file:

```
set_property IOSTANDARD value [get_ports port_name]
```

IBUF_LOW_PWR Attribute

The IBUF_LOW_PWR attribute allows an optional trade-off between performance and power. This attribute is set to TRUE by default, which implements the input buffer in the lower-power rather than the higher-performance mode.

RECOMMENDED: *For receivers that are expected to operate at data rates ≥1600 Mb/s, this attribute should be set to FALSE.*

The change in power between high-performance and low-power mode can be estimated using the Xilinx Power Estimator (XPE) spreadsheet tool (download at www.xilinx.com/power).

The IBUF_LOW_PWR attribute is applied to the I/O buffer instance and uses the following syntax in the XDC file:

```
set_property IBUF_LOW_PWR TRUE|FALSE [get_ports port_name]
```

Refer to the *UltraScale Architecture Libraries Guide* (UG974) [Ref 6] for information on accessing this attribute in UNISIM instantiation.

Output Slew Rate Attributes

Many attribute values provide the option of choosing the desired slew rate for I/O output buffers. For LVCMOS, LVTTL, SSTL, HSTL, and HSUL output buffers, including the differential versions, the desired slew rate can be specified with the SLEW attribute.

It might be important to specify FAST slew rate for high-performance applications such as high-frequency memory interfaces. However, faster slew rates can also lead to reflections or increased noise issues if not properly designed (such as with terminations, transmission line impedance continuity, and cross-coupling).

The allowed values for the SLEW attribute are SLOW, MEDIUM (HP I/O banks only), or FAST.

The SLEW attribute uses the following syntax in the XDC file:

```
set_property SLEW value [get_ports port_name]
```

By default, the slew rate for each output buffer is set to SLOW. This is the default used to minimize the power bus transients when switching non-critical signals.

Output Drive Strength Attributes

For LVCMOS and LVTTL output buffers, the desired drive strength (in mA) can be specified with the DRIVE attribute. The allowed values for the DRIVE attribute are shown in Table 1-11.

Table 1-11: **Allowed Values for the DRIVE Attribute**

Standard	HR I/O Bank Current Drive (mA)		HP I/O Bank Current Drive (mA)	
	Allowed Values	Default	Allowed Values	Default
LVCMOS12	4, 8, or 12	12	2, 4, 6, or 8	12(1)
LVCMOS15	4, 8, 12, or 16	12	2, 4, 6, 8, or 12	12
LVCMOS18	4, 8, 12, or 16	12	2, 4, 6, 8, or 12	12
LVCMOS25	4, 8, 12, or 16	12	N/A	N/A
LVCMOS33	4, 8, 12, or 16	12	N/A	N/A
LVTTL	4, 8, 12, or 16	12	N/A	N/A

Notes:

1. Change the drive setting from the default setting in the RTL or XDC file to one of the allowed values before running through the Vivado Design Suite.

The DRIVE attribute uses the following syntax in the XDC file:

```
set_property DRIVE drive_value [get_ports port_name]
```

PULLTYPE Attribute

Input buffers, 3-state outputs, and bidirectional buffers can have a weak pull-up resistor, a weak pull-down resistor, or a weak keeper circuit. PULLTYPE attribute has the following possible values.

- NONE
- PULLUP
- PULLDOWN
- KEEPER

This feature can be invoked by adding the following possible constraint values to the relevant net of the buffers. These attributes use the following syntaxes in the XDC file:

```
set_property PULLUP TRUE [get_ports port_name]
set_property PULLDOWN TRUE [get_ports port_name]
set_property KEEPER TRUE [get_ports port_name]
```

For more information on implementing these attributes on either individual I/Os or globally for all I/Os, see the pull-up, pull-down, and keeper descriptions in the *Vivado Design Suite Properties Reference Guide* (UG912) [Ref 7].

On-Die Termination Attribute (ODT)

The on-die termination (ODT) attribute supports split or single termination on the inputs of the HSTL, SSTL, POD, and HSUL standards. The advantage of using ODT over discrete resistors is that signal integrity is improved by completely removing the stub at the receiver.

The ODT attribute is used to define the value of the on-die termination at the input for both DCI and non-DCI versions of the standards supported.

The V_{CCO} of the I/O bank must be connected to the appropriate voltage level for the ODT attribute to perform as expected. See Table 1-72 for the V_{CCO} levels required for I/O standards.

The ODT attribute allowed values:

- RTT_40
- RTT_48
- RTT_60
- RTT_120
- RTT_240
- RTT_NONE

Note: Not all values are allowed for all applicable I/O standards and configurations.

The ODT attribute uses the following syntax in the XDC file:

```
set_property ODT value [get_ports port_name]
```

Source Termination Attribute (OUTPUT_IMPEDANCE)

The OUTPUT_IMPEDANCE attribute provides the option of choosing the driver impedance for HSTL, SSTL, HSUL, LVDCI, HSLVDCI, and POD drivers to match the characteristic impedance of the driven line. The OUTPUT_IMPEDANCE attribute is used to define the value of source termination at the driver for both DCI and non-DCI versions of the standards supported.

The OUTPUT_IMPEDANCE attribute allowed values:

- RDRV_40_40
- RDRV_48_48
- RDRV_60_60
- RDRV_NONE_NONE

Note: Not all values are allowed for all applicable I/O standards and configurations.

The XDC syntax for this attribute is:

```
set_property OUTPUT_IMPEDANCE value [get_ports port_name]
```

Differential Termination Attribute

The differential termination (DIFF_TERM or DIFF_TERM_ADV) attributes support the differential I/O standards when used as inputs. These attributes are used to turn the built-in, 100Ω, differential termination on or off. The on-chip input differential termination provides advantages over using a discrete resistor by completely removing the stub at the receiver, which improves signal integrity. Additionally it:

- Consumes less power than DCI termination
- Does not use VRP pins (DCI)

The V_{CCO} of the I/O bank must be connected to 1.8V for HP I/O banks and 2.5V for HR I/O banks to provide 100Ω of effective differential termination. DIFF_TERM and DIFF_TERM_ADV are only available for inputs and can *only* be used with the appropriate V_{CCO} voltage.

The DIFF_TERM_ADV attribute can be specified in the XDC constraints file. The DIFF_TERM attribute can be specified by setting the appropriate value in the generic map (VHDL) or in-line parameter (Verilog) of the instantiated primitives. Refer to the Vivado Design Suite HDL templates [Ref 4] [Ref 5]or the *UltraScale Architecture Libraries Guide* (UG974) [Ref 6] for the proper syntax for instantiating these primitives and setting the DIFF_TERM attribute.

Differential termination can either be invoked using the DIFF_TERM or DIFF_TERM_ADV attributes. DIFF_TERM is used if specified in the instantiated primitive. DIFF_TERM_ADV is used if specified in the XDC constraints file. DIFF_TERM values specified in the instantiated primitive gets translated to the corresponding DIFF_TERM_ADV setting in the XDC file.

The allowed values for the DIFF_TERM attribute are:

- DIFF_TERM = TRUE automatically maps to DIFF_TERM_ADV = TERM_100
- DIFF_TERM = FALSE automatically maps to DIFF_TERM_ADV = TERM_NONE (default)

The allowed values for DIFF_TERM_ADV attribute are:

- DIFF_TERM_ADV = TERM_NONE (default)
- DIFF_TERM_ADV = TERM_100

The DIFF_TERM_ADV attribute uses the following syntax in the XDC file:

```
set_property DIFF_TERM_ADV value [get_ports port_name]
```

Internal V_{REF}

The V_{REF} for I/O banks can be (optionally) generated inside UltraScale devices. Internal generation removes the need to provide for a particular V_{REF} supply rail on the printed circuit board (PCB). Consider this alternative when the UltraScale device is the only device on the board/system requiring a particular V_{REF} voltage supply level. The internally generated V_{REF} (INTERNAL_VREF) is sourced from the V_{CCO}.

In I/O banks, there is a one V_{REF} plane per bank and each bank can have the optional INTERNAL_VREF set to a single voltage level for the entire bank.

The constraint INTERNAL_VREF is assigned to one bank at a time.

Example 1: INTERNAL_VREF for Bank 84 using HSTL_II (1.5V), which requires a 0.75V reference voltage, uses the following constraint:

```
set_property INTERNAL_VREF 0.75 [get_iobanks 84]
```

Example 2: INTERNAL_VREF for Bank 65 using HSTL_II_18 (1.8V), which requires a 0.9V reference voltage, uses the following constraint.

```
set_property INTERNAL_VREF 0.90 [get_iobanks 65]
```

The rules for using INTERNAL_VREF are:

- One value of V_{REF} can be set for the bank.
- INTERNAL_VREF can only be set to the nominal reference voltage value of a given I/O standard.
- Valid settings of INTERNAL_VREF are listed. Not all values are supported in all types of banks:
  - 0.60
  - 0.675
  - 0.70
  - 0.75
  - 0.84
  - 0.90
- V_{REF} is a dedicated pin and cannot be used as a normal I/O pin even when INTERNAL_VREF is used.

The rules for combining I/O standards in the same bank also apply for INTERNAL_VREF. In HP I/O banks only, an internal V_{REF} scan feature is available for internal V_{REF} control. To use the V_{REF} scan feature in a bank, the INTERNAL_VREF must be set to the appropriate V_{REF} value for the I/O standards used in that bank. The internal V_{REF} scan is invoked using either the IBUFE3 or IOBUFE3 primitive in conjunction with the HPIO_VREF primitive.

Internal V_{REF} (INTERNAL_VREF and V_{REF} scan) cannot be combined with external V_{REF} usage within a bank.

DQS_BIAS

The DQS_BIAS attribute provides an optional DC bias at the inputs of certain pseudo-differential and true differential I/O standards.

The allowed values for the DQS_BIAS attribute for applicable I/O standards are:

- TRUE where DQS_BIAS = TRUE cannot be used in conjunction with the PULLTYPE attribute set to PULLUP, PULLDOWN, or KEEPER in the same port.
- FALSE (default)

The DQS_BIAS attribute should be set in the UNISIM instantiation. Refer to the *UltraScale Architecture Libraries Guide* (UG974) [Ref 6] for more information.

Transmitter Pre-Emphasis

The transmitter pre-emphasis (PRE_EMPHASIS) feature allows pre-emphasis on the drivers for certain I/O standards.

The allowed values for the PRE_EMPHASIS attribute are:

- PRE_EMPHASIS = RDRV_NONE (default)
- PRE_EMPHASIS = RDRV_240

The PRE_EMPHASIS attribute uses the following syntax in the XDC file:

```
set_property PRE_EMPHASIS value [get_ports port_name]
```

A typical pre-emphasis gain when using the PRE_EMPHASIS attribute in a DDR4 application with an OUTPUT_IMPEDANCE of 40Ω is listed in Table 1-12.

Table 1-12: **Typical Pre-emphasis Gain when Using the PRE_EMPHASIS Attribute in a DDR4 Application**

Attribute	Value	Estimated Gain (dB)
PRE_EMPHASIS (HP I/O banks) with an OUTPUT_IMPEDANCE of 40Ω.	RDRV_240	2.5

LVDS Transmitter Pre-Emphasis

The LVDS transmitter pre-emphasis (LVDS_PRE_EMPHASIS) feature allows pre-emphasis on the drivers for certain I/O standards.

The allowed values for the LVDS_PRE_EMPHASIS attribute are:

- LVDS_PRE_EMPHASIS = FALSE (Default)
- LVDS_PRE_EMPHASIS = TRUE

The LVDS_PRE_EMPHASIS attribute uses the following syntax in the XDC file:

```
set_property LVDS_PRE_EMPHASIS TRUE|FALSE [get_ports port_name]
```

A typical pre-emphasis gain when using the LVDS_PRE_EMPHASIS attribute is listed in Table 1-13.

Table 1-13: **Typical Pre-Emphasis Gain When Using the LVDS_PRE_EMPHASIS Attribute**

Attribute	Value	Estimated Gain (dB)
LVDS_PRE_EMPHASIS (HP I/O banks)	TRUE	4
LVDS_PRE_EMPHASIS (HR I/O banks)	TRUE	4

Receiver EQUALIZATION

The receiver equalization (EQUALIZATION) feature allows equalization at the receiver for certain I/O standards.

The allowed values for the EQUALIZATION attribute are:

HP I/O Banks

- EQ_LEVEL0
- EQ_LEVEL1
- EQ_LEVEL2
- EQ_LEVEL3
- EQ_LEVEL4
- EQ_NONE (Default)

HR I/O Banks

- EQ_LEVEL0
- EQ_LEVEL0_DC_BIAS
- EQ_LEVEL1

- EQ_LEVEL1_DC_BIAS
- EQ_LEVEL2
- EQ_LEVEL2_DC_BIAS
- EQ_LEVEL3
- EQ_LEVEL3_DC_BIAS
- EQ_LEVEL4
- EQ_LEVEL4_DC_BIAS
- EQ_NONE (Default)

IMPORTANT: *The HR I/O banks with _BIAS equalization values cannot be combined in the same port with the PULLTYPE attribute set to PULLUP, PULLDOWN, or KEEPER.*

The EQUALIZATION attribute uses the following syntax in the XDC file:

```
set_property EQUALIZATION value [get_ports port_name]
```

Typical AC gain for different values of EQUALIZATION for DDR4 and SGMII interfaces are listed in Table 1-14.

Table 1-14: **Typical AC Gain for Different Values of Equalization in DDR4 and SGMII Interfaces**

Attribute	Value	Estimated Gain (dB)
Equalization in DDR4 interfaces at 2.66 Gb/s (HP I/O banks)	EQ_LEVEL0	0
	EQ_LEVEL1	0.75
	EQ_LEVEL2	1.50
	EQ_LEVEL3	2.25
	EQ_LEVEL4	3.00
Equalization in SGMII interfaces at 1.25 Gb/s (HR and HP I/O banks)	EQ_LEVEL0/EQ_LEVEL0_DC_BIAS	0
	EQ_LEVEL1/EQ_LEVEL1_DC_BIAS	1.50
	EQ_LEVEL2/EQ_LEVEL2_DC_BIAS	3.00
	EQ_LEVEL3/EQ_LEVEL3_DC_BIAS	4.50
	EQ_LEVEL4/EQ_LEVEL4_DC_BIAS	6.00

Receiver OFFSET Control

The receiver offset control (OFFSET_CNTRL) feature allows offset cancellation in receivers for certain I/O standards to overcome offset variations due to process.

The valid values for the OFFSET_CNTRL attribute are:

- CNTRL_NONE (Default)
- FABRIC

  Note: OFFSET_CNTRL = MEM_CTRL is not a valid option

The OFFSET_CNTRL attribute uses the following syntax in the XDC file:

```
set_property OFFSET_CNTRL value [get_ports port_name]
```

To invoke the offset cancellation feature in an I/O bank, OFFSET_CNTRL must be set to FABRIC. The controls for offset cancellation are available using the IBUFE3, IBUFDSE3, IOBUFE3, or IOBUFDSE3 primitives.

VREF_CNTR

VREF_CNTR is an attribute specific to the receiver V_{REF} scan feature in HP I/O banks. It is used with the HPIO_VREF UNISIM primitive.

The valid values for VREF_CNTR attribute are:

- FABRIC_RANGE1 (POD standards)
- FABRIC_RANGE2 (other applicable standards)

FABRIC_RANGE1 is used with the POD standards and the FABRIC_RANGE2 is used with the other applicable standards when the receiver V_{REF} scan feature is invoked.

The VREF_CNTR attribute should be set in the UNISIM instantiation. Refer to the *UltraScale Architecture Libraries Guide* (UG974) [Ref 6] for more information.

I/O Resource VHDL/Verilog Examples

The VHDL and Verilog example syntaxes for instantiating the I/O resources are found in the Vivado Design Suite HDL templates [Ref 4] [Ref 5].

Supported I/O Standards and Terminations

The following sections provide an overview of the supported I/O standards and options. While most I/O supported standards specify a range of allowed voltages, this chapter records typical voltage values only. These standards are outlined in the Electronic Industry Alliance JEDEC specification [Ref 8].

LVTTL (Low Voltage TTL)

Table 1-15: **Available I/O Bank Type**

HR	HP
Available	N/A

LVTTL is a general-purpose EIA/JESD standard for 3.3V applications that uses a single-ended CMOS input buffer and a push-pull output buffer. This standard requires a 3.3V output source voltage (V_{CCO}), but does not require the use of a reference voltage (V_{REF}) or a termination voltage (V_{TT}). This standard is defined by JEDEC (JESD 8C.01) [Ref 8].

Sample circuits illustrating both unidirectional and bidirectional LVTTL termination techniques are shown in Figure 1-45 and Figure 1-46. These two diagrams show examples of source-series and parallel terminated topologies.

Figure 1-45 shows unidirectional terminated topologies.

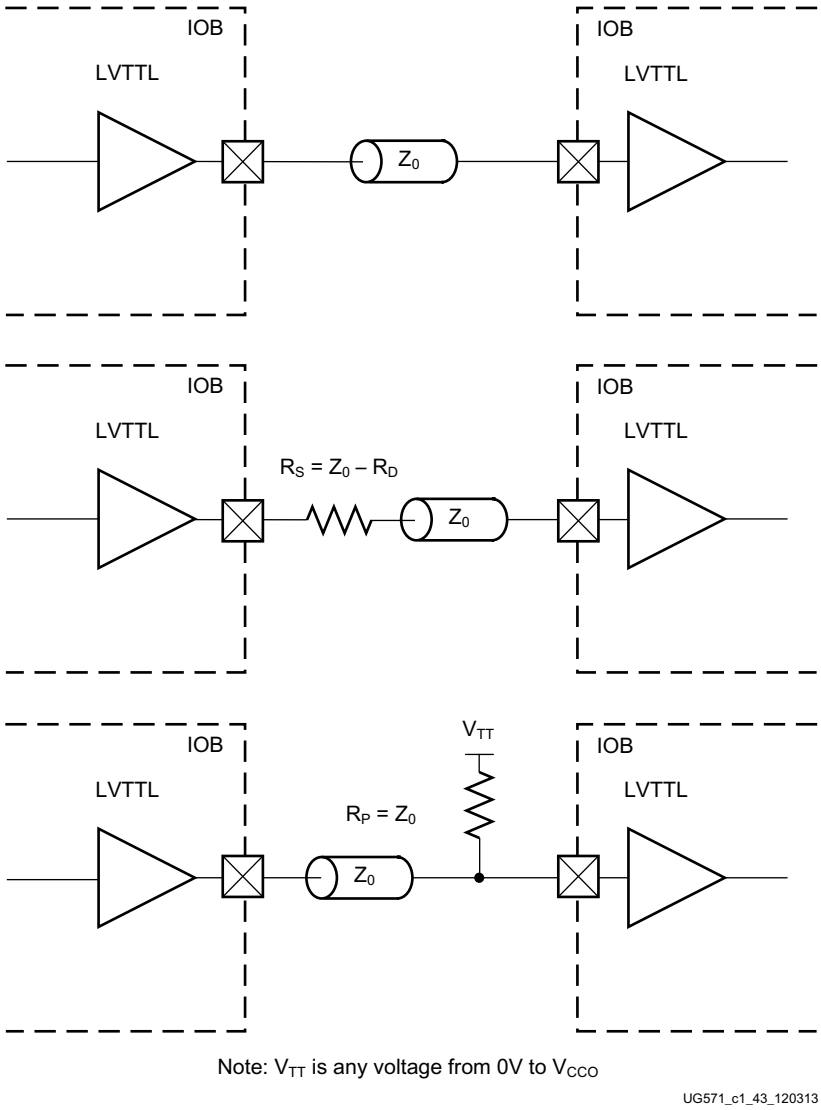

Figure 1-45: **LVTTL Unidirectional Termination**

Figure 1-46 shows a bidirectional, parallel-terminated topology.

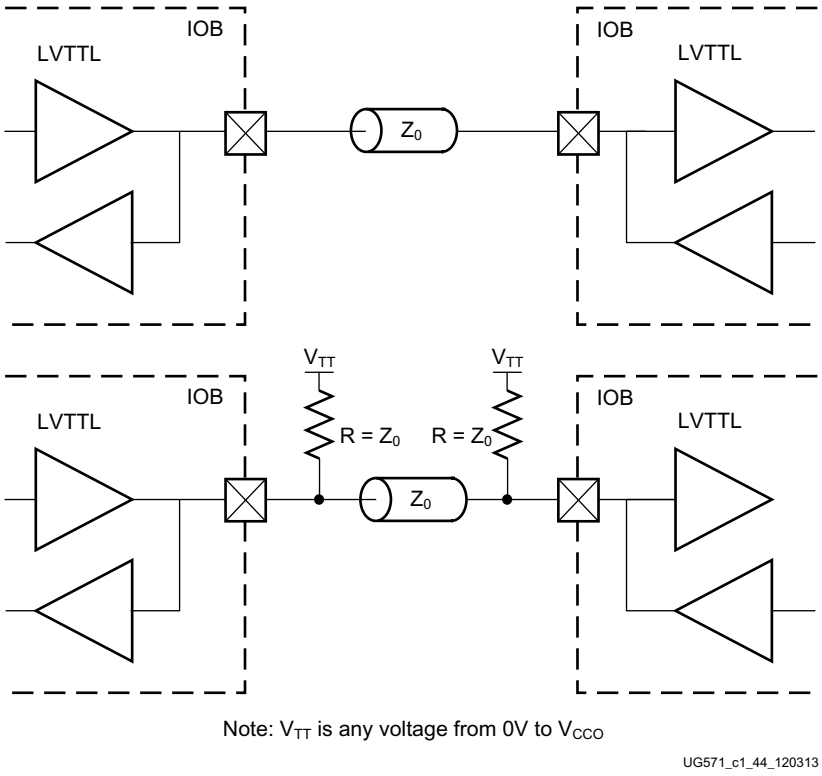

Figure 1-46: **LVTTL Bidirectional Termination**

Table 1-16 details the allowed attributes that can be applied to the LVTTL I/O standard. This standard is only available in the HR I/O banks.

Table 1-16: **Allowed Attributes for the LVTTL I/O Standards**

Attributes	Primitives		
	IBUF	OBUF/OBUFT/IOBUF	
		Allowed Values	Default
IOSTANDARD	LVTTL	LVTTL	
DRIVE	N/A	4, 8, 12, or 16	12
SLEW	N/A	FAST or SLOW	SLOW

LVCMOS (Low Voltage CMOS)

Table 1-17: **Available I/O Bank Type**

HR	HP
Available	Available

LVCMOS is a widely used switching standard implemented in CMOS transistors. This standard is defined by JEDEC (JESD 8C.01) [Ref 8]. The LVCMOS standards supported in UltraScale devices are: LVCMOS12, LVCMOS15, LVCMOS18, LVCMOS25, and LVCMOS33.

Sample circuits illustrating both unidirectional and bidirectional LVCMOS termination techniques are shown in Figure 1-47 and Figure 1-48. These two diagrams show examples of source-series and parallel terminated topologies.

Figure 1-47 shows unidirectional terminated topologies.

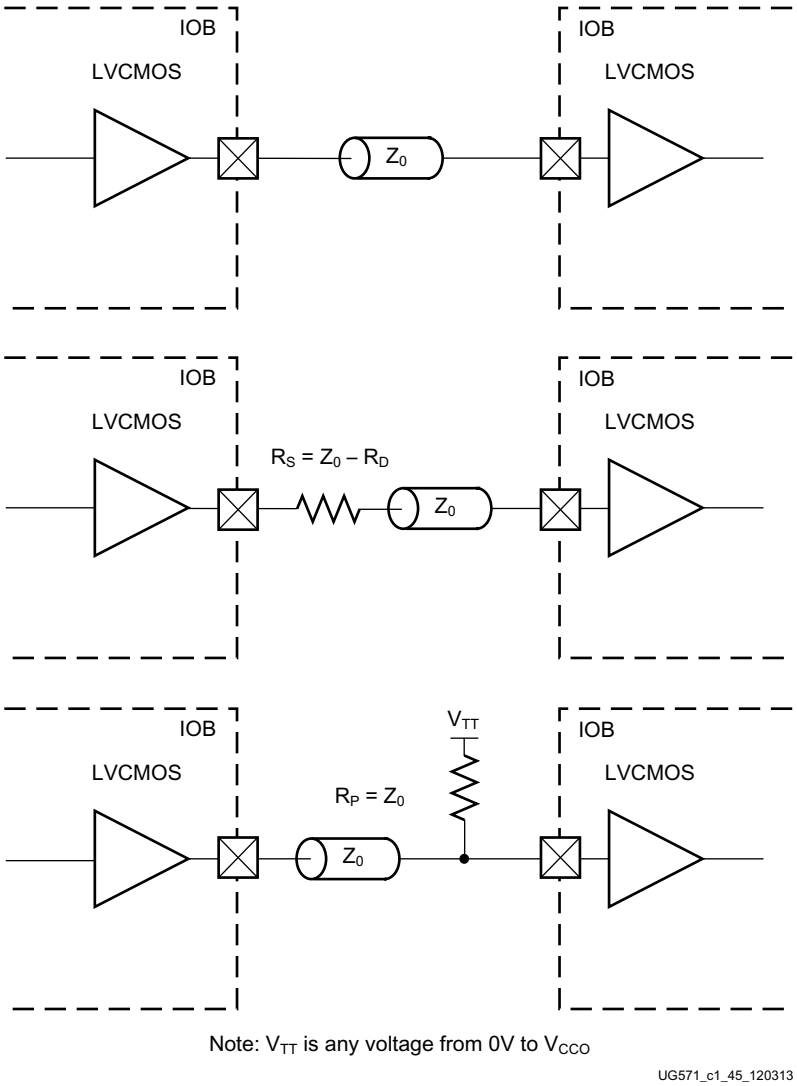

Figure 1-47: **LVCMOS Unidirectional Termination**

Figure 1-48 shows a bidirectional, parallel-terminated topology.

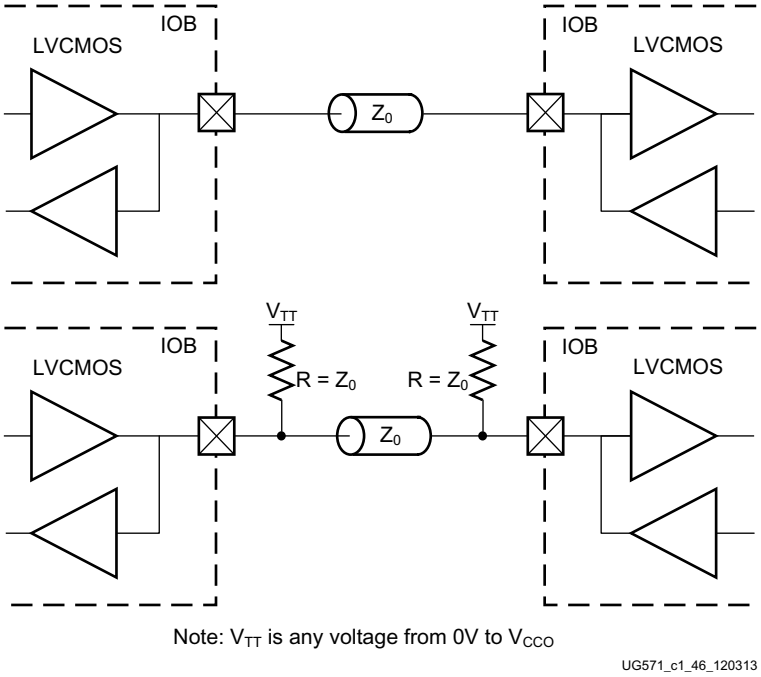

Figure 1-48: **LVCMOS Bidirectional Termination**

Table 1-18 details the allowed attributes that can be applied to the LVCMOS33 and LVCMOS25 I/O standards. These standards are only available in the HR I/O banks.

Table 1-18: **Allowed Attributes for the LVCMOS33 and LVCMOS25 I/O Standards**

Attributes	Primitives		
	IBUF	OBUF/OBUFT/IOBUF	
		Allowed Values	Default
IOSTANDARD	LVCMOS33, LVCMOS25	LVCMOS33, LVCMOS25	
DRIVE	N/A	4, 8, 12, or 16	12
SLEW	N/A	FAST or SLOW	SLOW

Table 1-19 details the allowed attributes that can be applied to the LVCMOS18 I/O standard. This standard is available in both the HR and HP I/O banks. For MOBILE DDR applications, the LVCMOS18 I/O standard is used with an 8 mA unterminated drive.

Table 1-19: **Allowed Attributes for the LVCMOS18 I/O Standard**

Attributes	Primitives				
	IBUF	OBUF/OBUFT/IOBUF			
		HP I/O Banks		HR I/O Banks	
		Allowed Values	Default	Allowed Values	Default
IOSTANDARD	LVCMOS18	LVCMOS18		LVCMOS18	
DRIVE	N/A	2, 4, 6, 8, 12	12	4, 8, 12, 16	12
SLEW	N/A	FAST, MEDIUM, SLOW	SLOW	FAST, SLOW	SLOW

Table 1-20 details the allowed attributes that can be applied to the LVCMOS15 I/O standard. This standard is available in both the HR and HP I/O banks.

Table 1-20: **Allowed Attributes for the LVCMOS15 I/O Standard**

Attributes	Primitives				
	IBUF	OBUF/OBUFT/IOBUF			
		HP I/O Banks		HR I/O Banks	
		Allowed Values	Default	Allowed Values	Default
IOSTANDARD	LVCMOS15	LVCMOS15		LVCMOS15	
DRIVE	N/A	2, 4, 6, 8, 12	12	4, 8, 12, 16	12
SLEW	N/A	FAST, MEDIUM, SLOW	SLOW	FAST, SLOW	SLOW

Table 1-21 details the allowed attributes that can be applied to the LVCMOS12 I/O standard. This standard is available in both the HR and HP I/O banks.

Table 1-21: **Allowed Attributes for the LVCMOS12 I/O Standard**

Attributes	Primitives				
	IBUF	OBUF/OBUFT/IOBUF			
		HP I/O Banks		HR I/O Banks	
		Allowed Values	Default	Allowed Values	Default
IOSTANDARD	LVCMOS12	LVCMOS12		LVCMOS12	
DRIVE	N/A	2, 4, 6, 8	12	4, 8, 12	12
SLEW	N/A	FAST, MEDIUM, SLOW	SLOW	FAST, SLOW	SLOW

LVDCI (Low-Voltage Digitally Controlled Impedance)

Table 1-22: **Available I/O Bank Type**

HR	HP
N/A	Available

Using these I/O buffers configures the outputs as controlled impedance drivers. The receiver of LVDCI is identical to a LVCMOS receiver. Some I/O standards, such as LVCMOS, must have a drive impedance that matches the characteristic impedance of the driven line. The HP I/O banks provide a controlled impedance output driver to provide series termination without external-source termination resistors.

Source termination is controlled using the OUTPUT_IMPEDANCE attribute. The exact value of the impedance is determined by the OUTPUT_IMPEDANCE attribute and an external 240Ω resistor on the VRP pin. The only valid value of this attribute for LVDCI standards is RDRV_48_48, which corresponds to a 48Ω setting.

Sample circuits illustrating both unidirectional and bidirectional topologies for a controlled impedance driver are shown in Figure 1-49 and Figure 1-50. The DCI I/O standards supporting a controlled impedance driver are: LVDCI_15 and LVDCI_18.

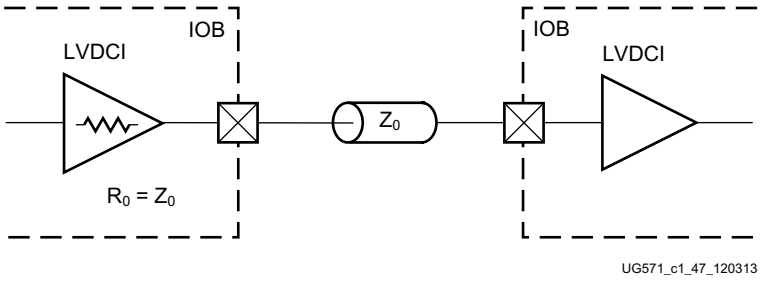

Figure 1-49: **Unidirectional Controlled Impedance Driver Topology**

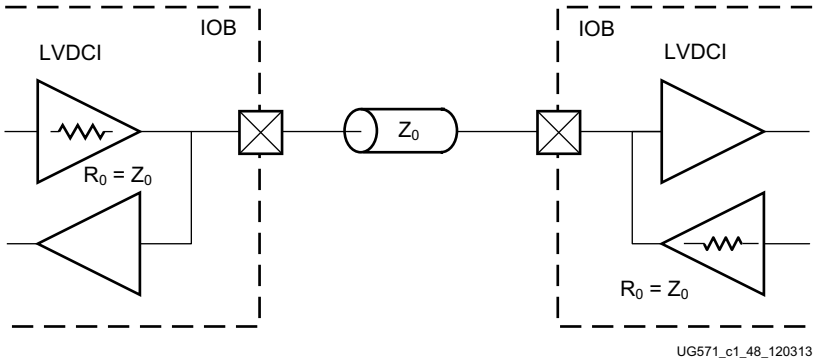

Figure 1-50: **Bidirectional Controlled Impedance Driver Topology**

Table 1-23 details the allowed attributes that can be applied to the LVDCI I/O standard. This standard is available in the HP I/O banks.

Table 1-23: **Allowed Attributes for the LVDCI I/O Standards**

Attributes	Primitives		
	IBUF	OBUF/OBUFT/IOBUF	
		Allowed Values	Default
IOSTANDARD	LVDCI_15, LVDCI_18	LVDCI_15, LVDCI_18	
SLEW	N/A	FAST, MEDIUM, SLOW	SLOW
OUTPUT_IMPEDANCE	N/A	RDRV_48_48	

HSLVDCI (High-Speed LVDCI)

Table 1-24: **Available I/O Bank Type**

HR	HP
N/A	Available

The driver is identical to LVDCI, while the input is identical to HSTL and SSTL. By using a V_{REF}-referenced input, HSLVDCI allows greater input sensitivity at the receiver than when using a single-ended LVCMOS-type receiver.

The HP I/O banks have a controlled impedance output driver to provide series termination without external-source termination resistors. The exact value of the impedance is set by the OUTPUT_IMPEDANCE attribute and an external 240Ω resistor on the VRP pin. The only valid value of the OUTPUT_IMPEDANCE attribute for HSLVDCI standards is RDRV_48_48, which corresponds to a 48Ω setting.

A sample circuit illustrating bidirectional termination techniques for an HSLVDCI controlled impedance driver is shown in Figure 1-51. The DCI I/O standards supporting a controlled impedance driver with a V_{REF} referenced input are: HSLVDCI_15 and HSLVDCI_18.

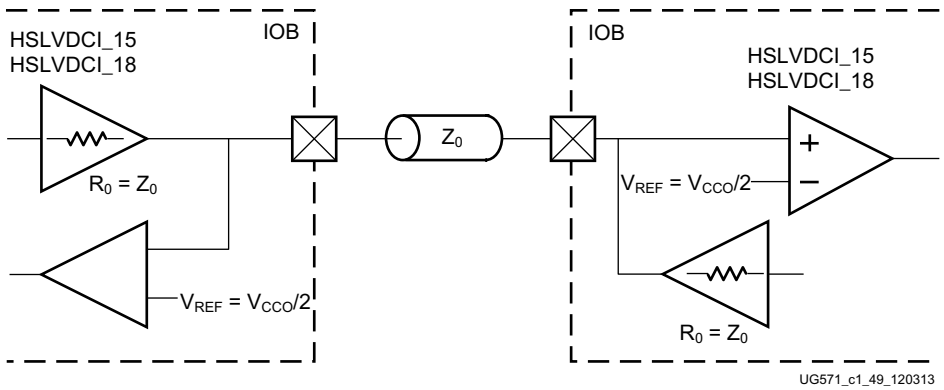

Figure 1-51: **HSLVDCI Controlled Impedance Driver with Bidirectional Termination**

For electrical specifications, see the LVDCI V_{OH} and V_{OL} entries in the UltraScale device data sheets [Ref 1].

Table 1-25 details the allowed attributes that can be applied to the HSLVDCI I/O standard. This standard is available in the HP I/O banks.

Table 1-25: **Allowed Attributes for the HSLVDCI I/O Standards**

Attributes	Primitives		
	IBUF	OBUF/OBUFT/IOBUF	
		Allowed Values	Default
IOSTANDARD	HSLVDCI_15, HSLVDCI_18	HSLVDCI_15, HSLVDCI_18	
SLEW	N/A	FAST, MEDIUM, SLOW	SLOW
OUTPUT_IMPEDANCE	N/A	RDRV_48_48	

HSTL (High-Speed Transceiver Logic)

The high-speed transceiver logic (HSTL) standard is a general purpose high-speed bus standard is defined by JEDEC (JESD8-6) [Ref 8]. To support clocking high-speed memory interfaces, differential versions are also available. The UltraScale architecture I/O supports class-I for the 1.2V version (in HP I/O banks) along with the 1.5V version and 1.8V versions (both HP and HR I/O banks), including the differential versions. Class-II supports the 1.5V version and 1.8V version (in HR I/O banks), including the differential versions. The differential versions of the standard require a differential amplifier input buffer and a push-pull output buffer. The HP I/O banks also support DCI versions.

HSTL_ I and HSTL_ I_18

Table 1-26: **Available I/O Bank Type**

HR	HP
Available	Available

HSTL_I and HSTL_ I_18 use $V_{CCO}/2$ as a parallel-termination voltage (V_{TT}).

Optional on-die untuned input split termination feature (ODT) provides thevenin equivalent resistance of 2R (where R = Z_0) to the $V_{CCO}/2$. The untuned on-die source termination feature (OUTPUT_IMPEDANCE) with optional 40Ω, 48Ω, or 60Ω of driver impedance is available in HP I/O banks. The default value of the driver output impedance is 48Ω.

HSTL_I_12

Table 1-27: **Available I/O Bank Type**

HR	HP
N/A	Available

HSTL_I_12 uses $V_{CCO}/2$ as a parallel-termination voltage (V_{TT}).

Optional on-die untuned input split termination feature (ODT) provides thevenin equivalent resistance of 2R (where R = Z_0) to the $V_{CCO}/2$. The untuned on-die source termination feature (OUTPUT_IMPEDANCE) with optional 40Ω, 48Ω, or 60Ω of driver impedance is available in HP I/O banks. The default value of the driver output impedance is 48Ω.

HSTL_ I_DCI, HSTL_I_DCI_12, and HSTL_ I_DCI_18

Table 1-28: **Available I/O Bank Type**

HR	HP
N/A	Available

HSTL_I_DCI, HSTL_I_DCI_12, and HSTL_I_DCI_18 provide on-chip split-Thevenin termination powered from V_{CCO}, using the ODT attribute, creating an equivalent parallel-termination voltage (V_{TT}) of $V_{CCO}/2$.

The source termination feature (OUTPUT_IMPEDANCE) provides the option of 40Ω, 48Ω, or 60Ω of tuned driver impedance in HP I/O banks. The default value of the driver output impedance is 48Ω.

HSTL_ II and HSTL_ II_18

Table 1-29: **Available I/O Bank Type**

HR	HP
Available	Not Available

HSTL_II and HSTL_II_18 use $V_{CCO}/2$ as a parallel-termination voltage (V_{TT}).

Optional on-die untuned input split termination feature (ODT) provides thevenin equivalent resistance of 2R (where R = Z_0) to the $V_{CCO}/2$.

DIFF_HSTL_I and DIFF_HSTL_I_18

Table 1-30: **Available I/O Bank Type**

HR	HP
Available	Available

Differential HSTL class-I pairs complementary single-ended HSTL_I type drivers with a differential receiver.

Optional on-die untuned input split termination feature (ODT) provides thevenin equivalent resistance of 2R (where R = Z_0) to the $V_{CCO}/2$. The untuned on-die source termination feature (OUTPUT_IMPEDANCE) with optional 40Ω, 48Ω, or 60Ω of driver impedance is available in HP I/O banks. The default value of the driver output impedance is 48Ω.

DIFF_HSTL_I_DCI and DIFF_HSTL_I_DCI_18

Table 1-31: **Available I/O Bank Type**

HR	HP
N/A	Available

Differential HSTL class-I pairs complementary single-ended HSTL_I type drivers with a differential receiver, including on-chip split-Thevenin termination using the ODT attribute.

The source termination feature (OUTPUT_IMPEDANCE) provides the option of 40Ω, 48Ω, or 60Ω of tuned driver impedance in HP I/O banks. The default value of the driver output impedance is 48Ω.

DIFF_HSTL_ II and DIFF_HSTL_II_18

Table 1-32: **Available I/O Bank Type**

HR	HP
Available	Not Available

Differential HSTL class-II pairs complementary single-ended HSTL_II type drivers with a differential receiver. Differential HSTL can also be used for differential clock and DQS signals in memory interface designs.

Optional on-die untuned input split termination feature (ODT) provides thevenin equivalent resistance of 2R (where R = Z_0) to the $V_{CCO}/2$.

DIFF_HSTL_I_12

Table 1-33: **Available I/O Bank Type**

HR	HP
Not Available	Available

Differential HSTL class-I pairs complementary single-ended HSTL_I_12 type drivers with a differential receiver.

Optional on-die untuned input split termination feature (ODT) provides thevenin equivalent resistance of 2R (where R = Z_0) to the V_{CCO}/2.The untuned on-die source termination feature (OUTPUT_IMPEDANCE) with optional 40Ω, 48Ω, or 60Ω of driver impedance is available in HP I/O banks. The default value of the driver output impedance is 48Ω.

DIFF_HSTL_I_12_DCI

Table 1-34: **Available I/O Bank Type**

HR	HP
Not Available	Available

Differential HSTL class-I pairs complementary single-ended HSTL_I_12 type drivers with a differential receiver, including on-chip split-Thevenin termination using the ODT attribute. The source termination feature (OUTPUT_IMPEDANCE) provides the option of 40Ω, 48Ω, or 60Ω of tuned driver impedance in HP I/O banks. The default value of the driver output impedance is 48Ω.

HSTL Class I (1.2V, 1.5V, or 1.8V)

Figure 1-52 shows a sample circuit illustrating a termination technique for HSTL class-I for the 1.2V, 1.5V, or 1.8V versions. In a specific circuit, all drivers and receivers must be at the same voltage level (1.2V, 1.5V or 1.8V); they are not interchangeable. Only HP I/O banks support the DCI standards.

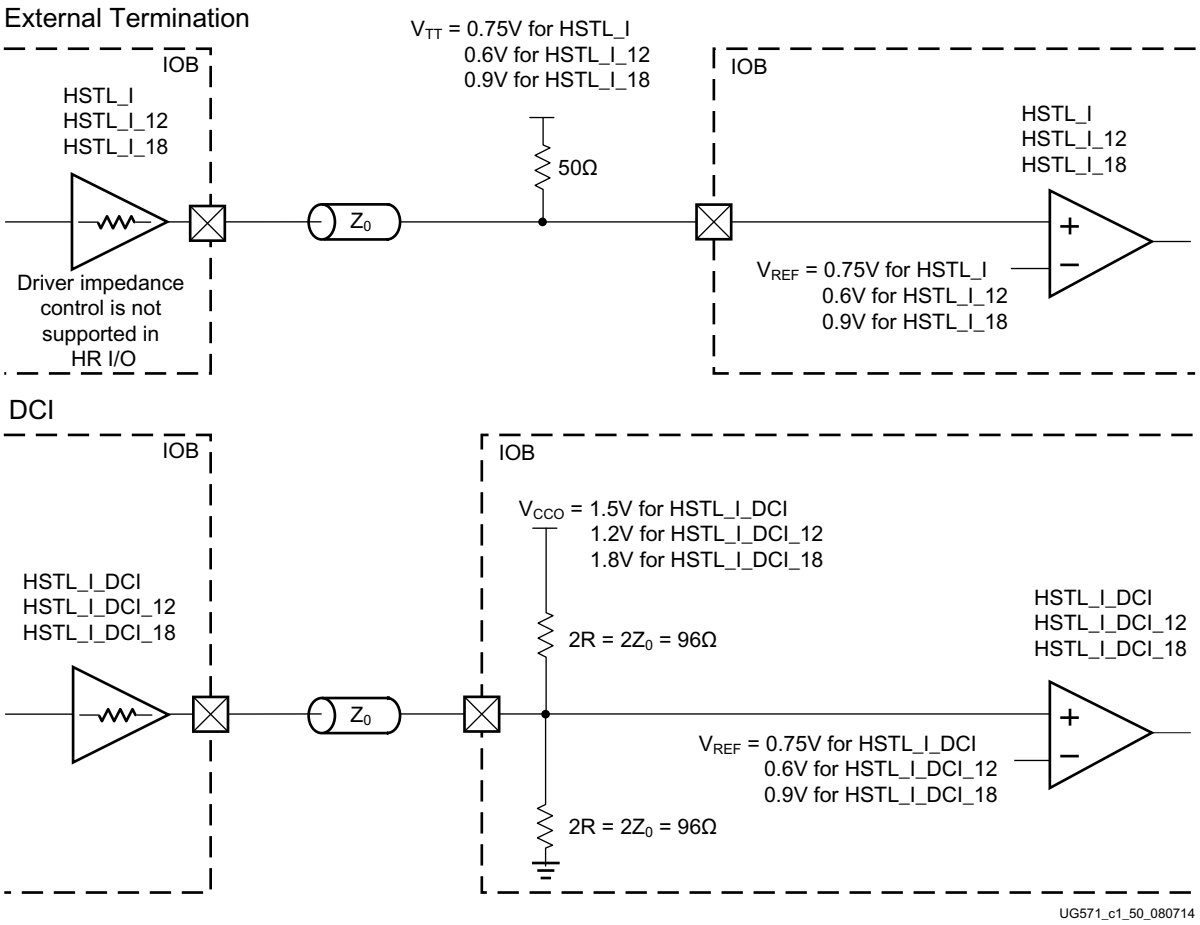

Figure 1-52: **HSTL Class I (1.2V, 1.5V, or 1.8V) Unidirectional Termination**

Figure 1-53 shows a sample circuit illustrating a termination technique for HSTL class-I for the 1.2V, 1.5V, or 1.8V versions in a bidirectional configuration. In a specific circuit, all drivers and receivers must be at the same voltage level (1.2V, 1.5V, or 1.8V); they are not interchangeable. Only HP I/O banks support the DCI standards.

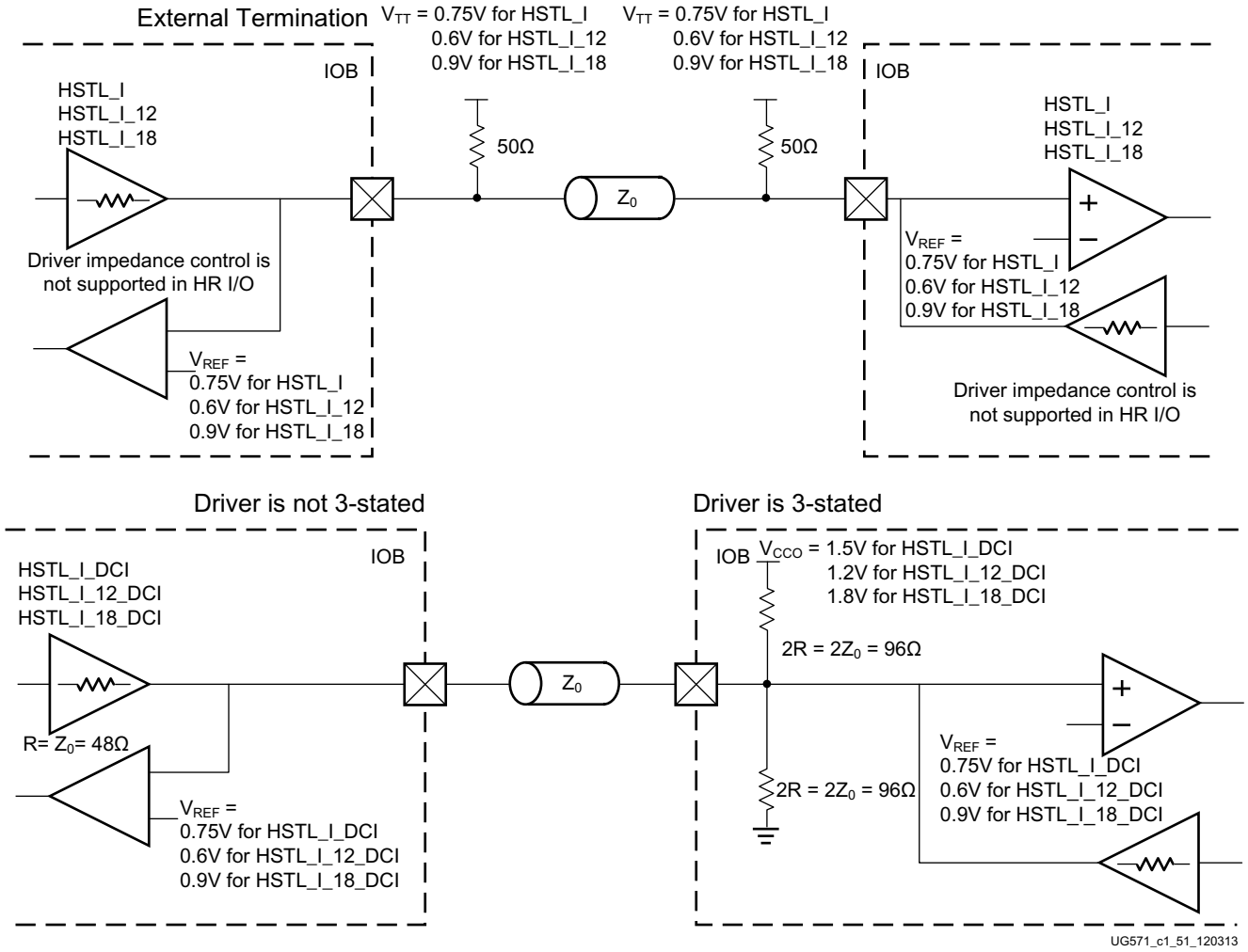

Figure 1-53: **HSTL Class I (1.2V, 1.5V, or 1.8V) Bidirectional Termination**

Differential HSTL Class I

Figure 1-54 shows a sample circuit illustrating a termination technique for differential HSTL class-I (1.2V, 1.5V, or 1.8V) with unidirectional termination. In a specific circuit, all drivers and receivers must be at the same voltage level (1.2V, 1.5V, or 1.8V); they are not interchangeable.

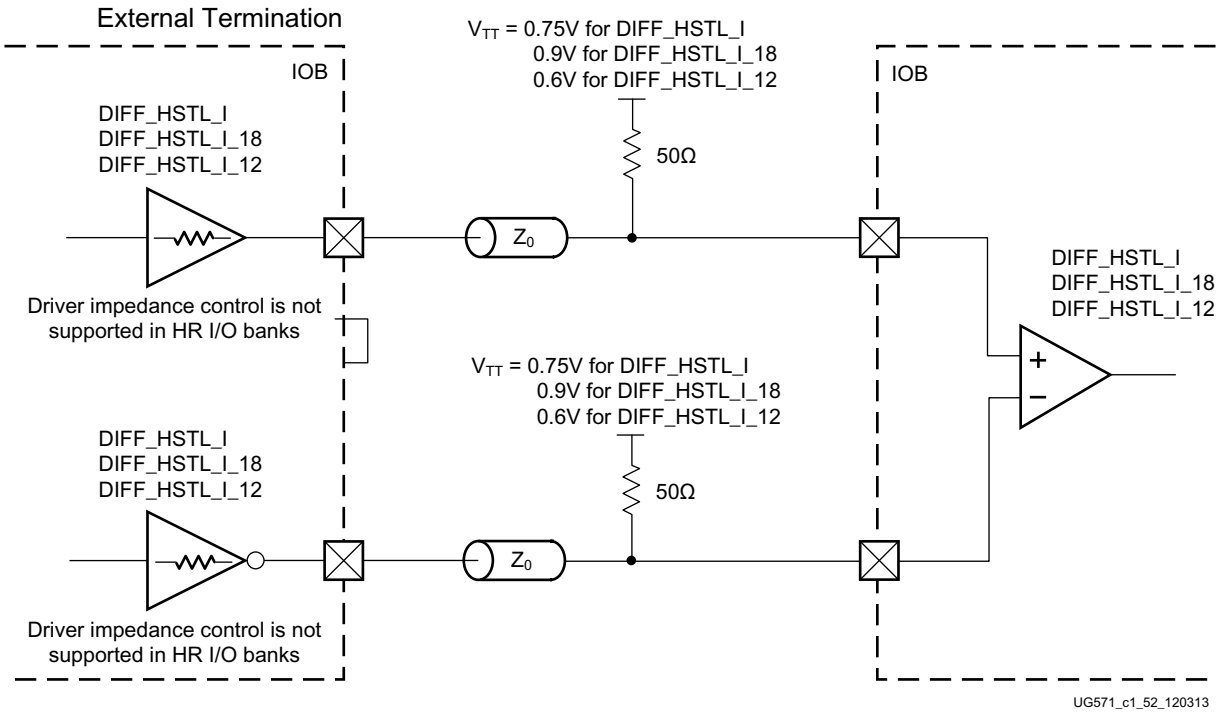

Figure 1-54: **Differential HSTL Class I (1.2V, 1.5V, or 1.8V) Unidirectional Termination**

Figure 1-55 shows a sample circuit illustrating a termination technique for differential HSTL class-I (1.2V, 1.5V, or 1.8V) with bidirectional termination. In a specific circuit, all drivers and receivers must be at the same voltage level (1.2V, 1.5V, or 1.8V); they are not interchangeable.

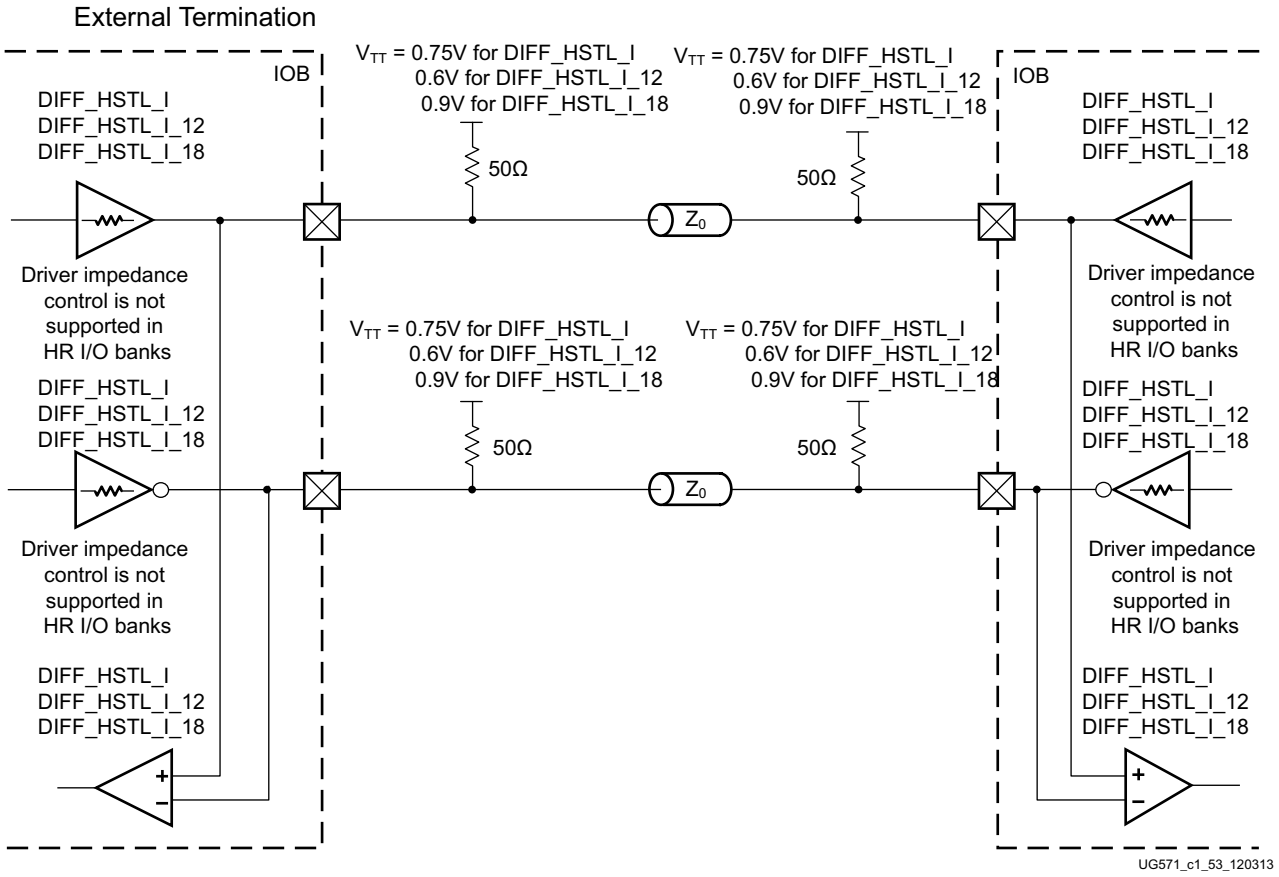

Figure 1-55: **Differential HSTL Class I (1.2V, 1.5V, or 1.8V) Bidirectional Termination**

Figure 1-56 shows a sample circuit illustrating a termination technique for differential HSTL class-I (1.2V, 1.5V, or 1.8V) with unidirectional DCI termination. In a specific circuit, all drivers and receivers must be at the same voltage level (1.2V, 1.5V, or 1.8V); they are not interchangeable. Only HP I/O banks support these DCI standards.

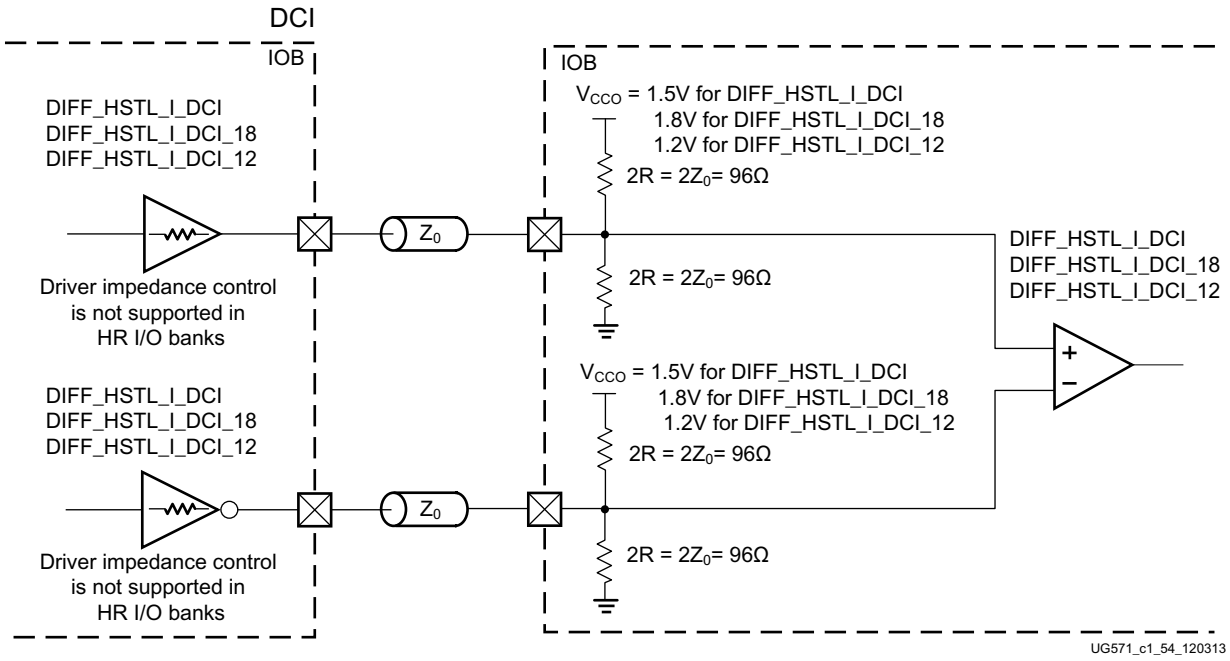

Figure 1-56: **Differential HSTL Class I (1.2V, 1.5V, or 1.8V) DCI Unidirectional Termination**

Figure 1-57 shows a sample circuit illustrating a termination technique for differential HSTL class-I (1.2V, 1.5V, or 1.8V) with bidirectional DCI termination. In a specific circuit, all drivers and receivers must be at the same voltage level (1.2V, 1.5V, or 1.8V); they are not interchangeable. Only HP I/O banks support these DCI standards.

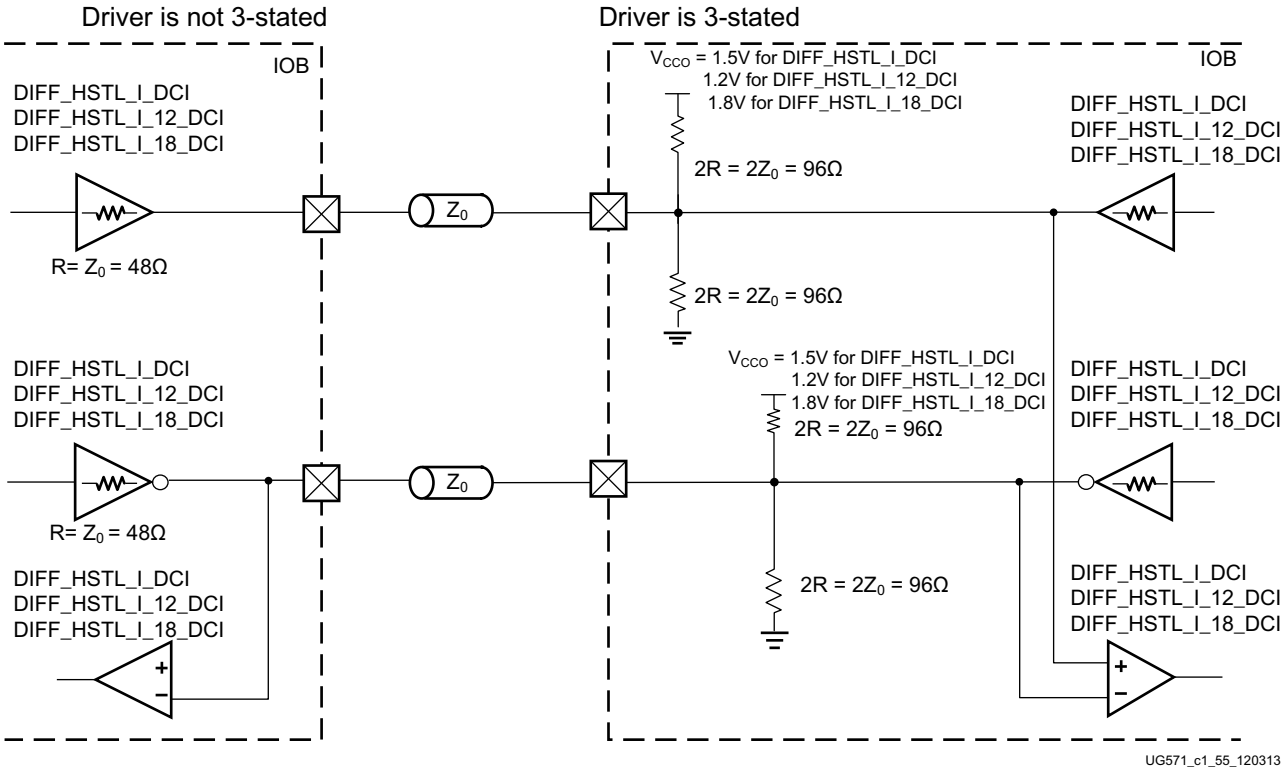

Figure 1-57: **Differential HSTL Class I (1.2V, 1.5V, or 1.8V) DCI Bidirectional Termination**

HSTL Class II

Figure 1-58 shows a sample circuit illustrating a termination technique for HSTL class-II (1.5V or 1.8V) with unidirectional termination. In a specific circuit, all drivers and receivers must be at the same voltage level (1.5V or 1.8V); they are not interchangeable. Only HR I/O banks support the class-II standards.

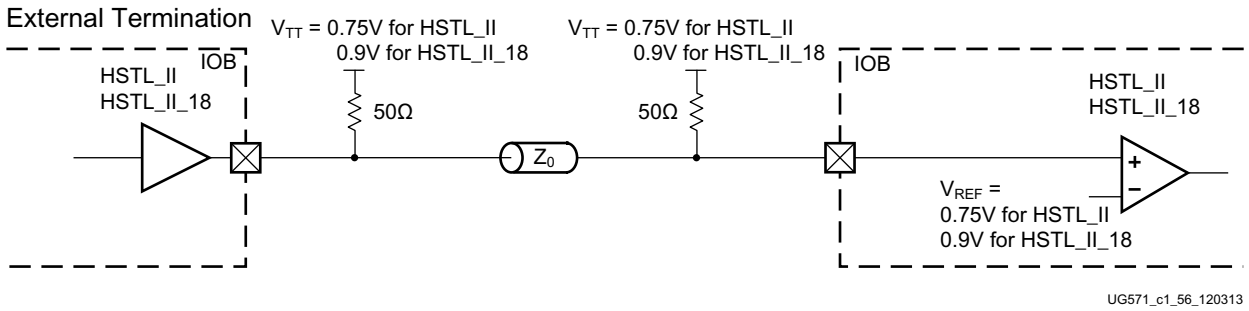

Figure 1-58: **HSTL Class II (1.5V or 1.8V) Unidirectional Termination**

Figure 1-59 shows a sample circuit illustrating a termination technique for HSTL class-II (1.5V or 1.8V) with bidirectional termination. In a specific circuit, all drivers and receivers must be at the same voltage level (1.5V or 1.8V); they are not interchangeable.

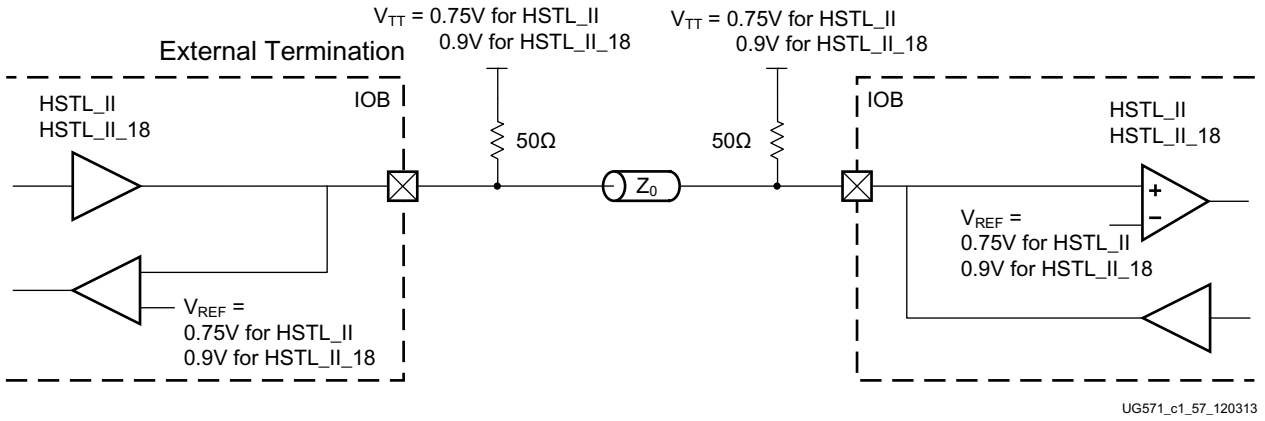

Figure 1-59: **HSTL Class II (1.5V or 1.8V) Bidirectional Termination**

Differential HSTL Class II

Figure 1-60 shows a sample circuit illustrating a termination technique for differential HSTL (1.5V or 1.8V) with unidirectional termination. In a specific circuit, all drivers and receivers must be at the same voltage level (1.5V or 1.8V); they are not interchangeable. Only HR I/O banks support the class-II standards.

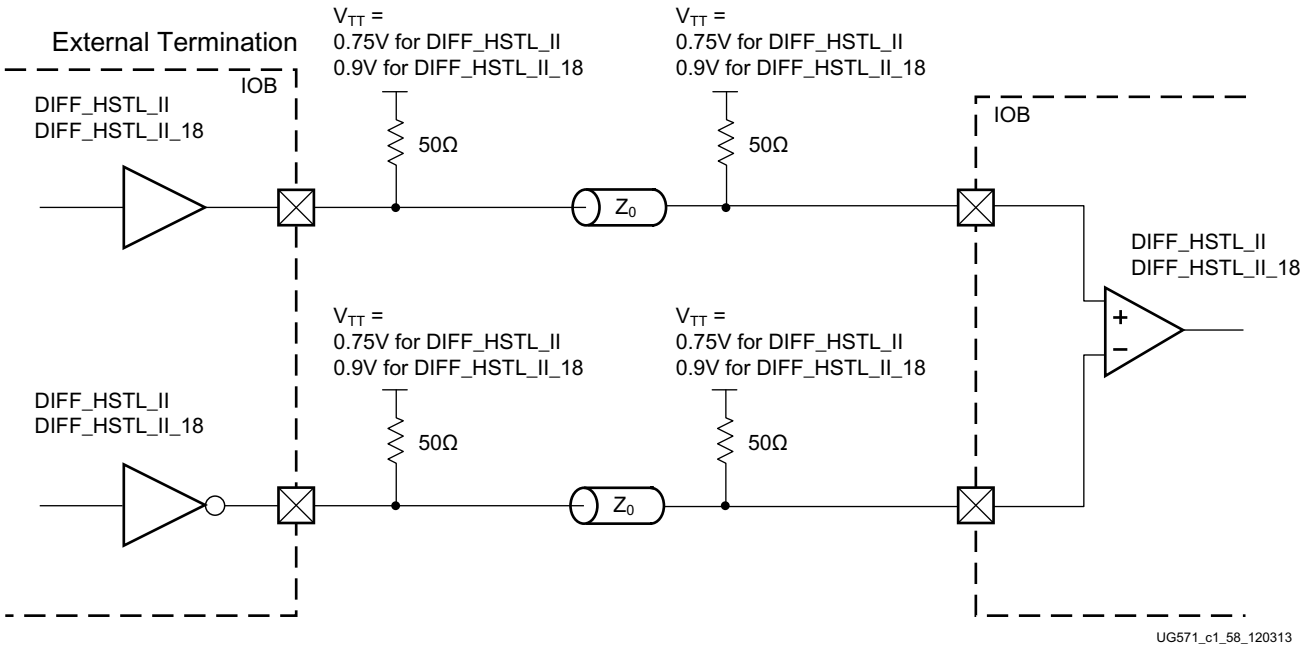

Figure 1-60: **Differential HSTL (1.5V or 1.8V) Unidirectional Termination**

Figure 1-61 shows a sample circuit illustrating a termination technique for differential HSTL class-II (1.5V or 1.8V) with bidirectional termination. In a specific circuit, all drivers and receivers must be at the same voltage level (1.5V or 1.8V); they are not interchangeable.

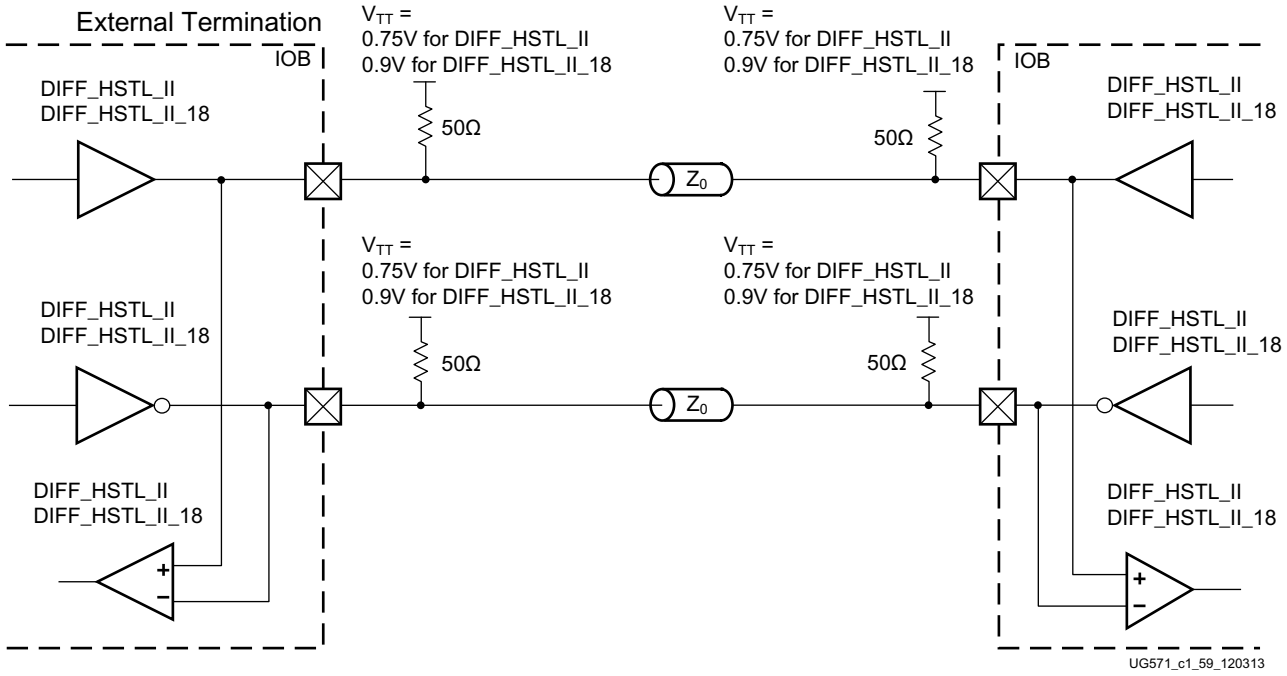

Figure 1-61: **Differential HSTL Class II (1.5V or 1.8V) Bidirectional Termination**

Table 1-35 and Table 1-36 list the supported attributes for the HSTL I/O standards.

Table 1-35: **HSTL Class I Allowed Attributes**

Attributes	IBUF/IBUFE3/IBUFDS/IBUFDSE3				OBUF/OBUFT				IOBUF/IOBUFE3/IOBUFDS/IOBUFDSE3			
	HP I/O		HR I/O		HP I/O		HR I/O		HP I/O		HR I/O	
	Allowed Values	Default	Allowed Values	Default	Allowed Values	Default	Allowed Values	Default	Allowed Values	Default	Allowed Values	Default
IOSTANDARD	HSTL_I HSTL_I_12 HSTL_I_18		HSTL_I HSTL_I_18		HSTL_I HSTL_I_12 HSTL_I_18		HSTL_I HSTL_I_18		HSTL_I HSTL_I_12 HSTL_I_18		HSTL_I HSTL_I_18	
SLEW	N/A		N/A		FAST MEDIUM SLOW	SLOW	FAST SLOW	SLOW	FAST MEDIUM SLOW	SLOW	FAST SLOW	SLOW
ODT	RTT_40 RTT_48 RTT_60 RTT_NONE	RTT_NONE	RTT_40 RTT_48 RTT_60 RTT_NONE	RTT_NONE	N/A		N/A		RTT_40 RTT_48 RTT_60 RTT_NONE(1)	RTT_NONE	RTT_40 RTT_48 RTT_60 RTT_NONE	RTT_NONE
OUTPUT_ IMPEDANCE	N/A		N/A		RDRV_40_40 RDRV_48_48 RDRV_60_60	RDRV_48_48	N/A		RDRV_40_40 RDRV_48_48 RDRV_60_60(1)	RDRV_48_48	N/A	
IOSTANDARD	HSTL_I_DCI HSTL_I_DCI_12 HSTL_I_DCI_18		N/A		HSTL_I_DCI HSTL_I_DCI_12 HSTL_I_DCI_18		N/A		HSTL_I_DCI HSTL_I_DCI_12 HSTL_I_DCI_18		N/A	
SLEW	N/A		N/A		FAST MEDIUM SLOW	SLOW	N/A		FAST MEDIUM SLOW	SLOW	N/A	
ODT	RTT_40 RTT_48 RTT_60(2)	RTT_48	N/A		N/A		N/A		RTT_40 RTT_48 RTT_60(1)(2)	RTT_48	N/A	
OUTPUT_ IMPEDANCE	N/A		N/A		RDRV_40_40 RDRV_48_48 RDRV_60_60	RDRV_48_48	N/A		RDRV_40_40 RDRV_48_48 RDRV_60_60(1)	RDRV_48_48	N/A	

Table 1-35: **HSTL Class I Allowed Attributes *(Cont'd)***

Attributes	IBUF/IBUFE3/IBUFDS/IBUFDSE3				OBUF/OBUFT				IOBUF/IOBUFE3/IOBUFDS/IOBUFDSE3			
	HP I/O		HR I/O		HP I/O		HR I/O		HP I/O		HR I/O	
	Allowed Values	Default	Allowed Values	Default	Allowed Values	Default	Allowed Values	Default	Allowed Values	Default	Allowed Values	Default
IOSTANDARD	DIFF_HSTL_I DIFF_HSTL_I_12 DIFF_HSTL_I_18		DIFF_HSTL_I DIFF_HSTL_I_18		DIFF_HSTL_I DIFF_HSTL_I_12 DIFF_HSTL_I_18		DIFF_HSTL_I DIFF_HSTL_I_18		DIFF_HSTL_I DIFF_HSTL_I_12 DIFF_HSTL_I_18		DIFF_HSTL_I DIFF_HSTL_I_18	
SLEW	N/A		N/A		FAST MEDIUM SLOW	SLOW	FAST SLOW	SLOW	FAST MEDIUM SLOW	SLOW	FAST SLOW	SLOW
ODT	RTT_40 RTT_48 RTT_60 RTT_NONE	RTT_NONE	RTT_40 RTT_48 RTT_60 RTT_NONE	RTT_NONE	N/A		N/A		RTT_40 RTT_48 RTT_60 RTT_NONE(1)	RTT_NONE	RTT_40 RTT_48 RTT_60 RTT_NONE	RTT_NONE
OUTPUT_ IMPEDANCE	N/A		N/A		RDRV_40_40 RDRV_48_48 RDRV_60_60	RDRV_48_48	N/A		RDRV_40_40 RDRV_48_48 RDRV_60_60(1)	RDRV_48_48	N/A	
IOSTANDARD	DIFF_HSTL_I_DCI DIFF_HSTL_I_DCI_12 DIFF_HSTL_I_DCI_18		N/A		DIFF_HSTL_I_DCI DIFF_HSTL_I_DCI_12 DIFF_HSTL_I_DCI_18		N/A		DIFF_HSTL_I_DCI DIFF_HSTL_I_DCI_12 DIFF_HSTL_I_DCI_18		N/A	
SLEW	N/A		N/A		FAST MEDIUM SLOW	SLOW	N/A		FAST MEDIUM SLOW	SLOW	N/A	
ODT	RTT_40 RTT_48 RTT_60(2)	RTT_48	N/A		N/A		N/A		RTT_40 RTT_48 RTT_60(1)(2)	RTT_48	N/A	
OUTPUT_ IMPEDANCE	N/A		N/A		RDRV_40_40 RDRV_48_48 RDRV_60_60	RDRV_48_48	N/A		RDRV_40_40 RDRV_48_48 RDRV_60_60(1)	RDRV_48_48	N/A	

Notes:

1. The allowed bidirectional configuration combinations for driver output impedance (OUTPUT_IMPEDANCE) and ODT are listed in Table 1-36.
2. ODT = RTT_NONE is not a valid setting for DCI I/O standards.

Table 1-36: **Only Allowed Combinations for Bidirectional Configurations**

OUTPUT_IMPEDANCE	ODT
RDRV_40_40 (40Ω)	RTT_40
RDRV_40_40 (40Ω)	RTT_60
RDRV_40_40 (40Ω)	RTT_NONE
RDRV_48_48 (48Ω)	RTT_48
RDRV_48_48 (48Ω)	RTT_NONE
RDRV_60_60 (60Ω)	RTT_40
RDRV_60_60 (60Ω)	RTT_60
RDRV_60_60 (60Ω)	RTT_NONE

Table 1-37 lists the supported attributes for the HSTL Class-II I/O standards.

Table 1-37: **HSTL Class II Allowed Attributes**

Attributes	IBUF/IBUFDS			OBUF/OBUFT			IOBUF/IOBUFDS		
	HP I/O	HR I/O		HP I/O	HR I/O		HP I/O	HR I/O	
		Allowed Values	Default		Allowed Values	Default		Allowed Values	Default
IOSTANDARD	N/A	HSTL_II HSTL_II_18		N/A	HSTL_II HSTL_II_18		N/A	HSTL_II HSTL_II_18	
SLEW	N/A	N/A		N/A	FAST SLOW	SLOW	N/A	FAST SLOW	SLOW
ODT	N/A	RTT_40 RTT_48 RTT_60 RTT_NONE	RTT_NONE	N/A	N/A		N/A	RTT_40 RTT_48 RTT_60 RTT_NONE	RTT_NONE
IOSTANDARD	N/A	DIFF_HSTL_II DIFF_HSTL_II_18		N/A	DIFF_HSTL_II DIFF_HSTL_II_18		N/A	DIFF_HSTL_II DIFF_HSTL_II_18	
SLEW	N/A	N/A		N/A	FAST SLOW	SLOW	N/A	FAST SLOW	SLOW
ODT	N/A	RTT_40 RTT_48 RTT_60 RTT_NONE	RTT_NONE	N/A	N/A		N/A	RTT_40 RTT_48 RTT_60 RTT_NONE	RTT_NONE

SSTL (Stub-Series Terminated Logic)

The Stub-Series Terminated Logic (SSTL) for 1.8V (SSTL18), 1.5V (SSTL15), and 1.35V (SSTL135) are I/O standards used for general purpose memory buses.

While example termination techniques are discussed in this section, the optimal termination schemes for a given memory interface are determined using signal-integrity analysis of the actual PCB topology including the memory devices used, the board layout, and transmission line impedances. Xilinx provides both IBIS model files and encrypted HSPICE model files for all of the I/O standards. These SSTL standards are supported for both single-ended signaling and differential signaling. The differential versions use a true differential amplifier input buffer and complementary push-pull output buffers. The DCI versions of these standards are the preferred I/O standards to use for memory interfaces implemented in the HP I/O banks. The uncalibrated split termination (using the ODT attributes) is recommended for interfaces implemented without the DCI standards.

SSTL18 is defined by the JEDEC standard JESD8-15 [Ref 8], and is used for DDR2 SDRAM interfaces. For some topologies (such as short, point-to-point interfaces), the class-I driver can result in reduced overshoot and better signal integrity.

SSTL18 class-I is available in both the HP and HR I/O banks. Both HP and HR I/O banks provide ODT attributes for untuned internal parallel split-termination resistors for the non-DCI versions of these standards. In addition, the source termination feature (OUTPUT_IMPEDANCE) provides the option of 40Ω, 48Ω, or 60Ω tuned driver impedance in HP I/O banks in both DCI and non-DCI versions. The driver output impedance is set to a default of 40Ω. The optimal drive and termination scheme for any new design is determined through careful signal-integrity analysis. SSTL18 class-II is available in HR I/O banks. HR I/O banks provide the option of ODT attributes for untuned internal parallel split-termination resistors for the standard.

SSTL15 is used for DDR3 SDRAM interfaces and is roughly defined (not by name) in the JEDEC standard JESD79-3E [Ref 8]. For this standard, the full-strength driver (SSTL15) is available in both the HP and HR I/O banks. A weaker, reduced-strength driver, designated by an R in the standard name (SSTL15_R), is available in the HR I/O banks. For some topologies (such as short point-to-point interfaces), the reduced-strength driver can result in reduced overshoot and better signal integrity. The HP I/O banks provide DCI options for tuned internal parallel split-termination resistors. HP and HR I/O banks provide options for untuned internal parallel split-termination resistors (using the ODT attributes). In addition, the source termination feature (OUTPUT_IMPEDANCE) provides the option of 40Ω, 48Ω, or 60Ω tuned driver impedance in HP I/O banks in both DCI and non-DCI versions. The driver output impedance is set to a default of 40Ω. The optimal drive and termination scheme for any new design is determined through careful signal-integrity analysis.

SSTL135 is used for DDR3L SDRAM interfaces and is roughly defined (not by name) in the JEDEC standard JESD79-3-1 [Ref 8]. For this standard, the full-strength driver (SSTL135) is available in both the HP and HR I/O banks. A weaker, reduced-strength driver, designated by an R in the standard name (SSTL135_R), is available in the HR I/O banks. For some

topologies (such as short point-to-point interfaces), the reduced-strength driver can result in reduced overshoot and better signal integrity.

The HP I/O banks also provide DCI options for tuned internal parallel split-termination resistors. HP and HR I/O banks also provide options for untuned internal parallel split-termination resistors (using the ODT attributes). In addition, the source termination feature (OUTPUT_IMPEDANCE) provides the option of 40Ω, 48Ω, or 60Ω tuned driver impedance in HP I/O banks in both DCI and non-DCI versions. The driver output impedance is set to a default of 40Ω. The optimal drive and termination scheme for any new design is determined through careful signal-integrity analysis.

SSTL12 supports Micron's next-generation RLDRAM3 memory. The DCI option is available to improve the signal integrity through the use of tuned internal split-termination resistors in HP I/O banks. HR and HP I/O banks also provide the ODT attribute options for untuned internal parallel split-termination resistors. In addition, the source termination feature (OUTPUT_IMPEDANCE) provides the option of 40Ω, 48Ω, or 60Ω tuned driver impedance in HP I/O banks in both DCI and non-DCI versions. The driver output impedance is set to a default of 40Ω. The optimal drive and termination scheme for any new design is determined through careful signal-integrity analysis.

SSTL18_I, DIFF_SSTL18_I

Table 1-38: **Available I/O Bank Type**

HR	HP
Available	Available

Class-I drivers can be preferred for short, point-to-point board topologies. Parallel end-termination resistors (commonly 50Ω) to V_{TT} = (V_{CCO}/2) are typically placed on the board close to any receiver. Optional on-die untuned input split termination feature (ODT) provides thevenin equivalent resistance of 2R (where R = Z_0) to the V_{CCO}/2. The untuned on-die source termination feature (OUTPUT_IMPEDANCE) provides the option of 40Ω, 48Ω, or 60Ω of driver impedance in HP I/O banks. The driver output impedance is set to a default of 40Ω. The differential (DIFF_) version uses complementary single-ended drivers for outputs, and differential receivers for inputs.

SSTL18_I_DCI, DIFF_SSTL18_I_DCI

Table 1-39: **Available I/O Bank Type**

HR	HP
N/A	Available

Class-I drivers can be preferred for short, point-to-point board topologies. DCI provides tuned internal parallel split-termination resistors that are always present. The value of the ODT attributes represents the Thevenin equivalent resistance of 2R (where R = Z_0) to the $V_{CCO}/2$ mid-point level. The source termination feature (OUTPUT_IMPEDANCE) provides the option of 40Ω, 48Ω, or 60Ω tuned driver impedance in HP I/O banks. The driver output impedance is set to a default of 40Ω. The differential (DIFF_) version uses complementary single-ended drivers for outputs, and differential receivers for inputs.

SSTL18_II, SSTL15_R, SSTL135_R, DIFF_SSTL18_II, DIFF_SSTL15_R, DIFF_SSTL135_R

Table 1-40: **Available I/O Bank Type**

HR	HP
Available	Not Available

Parallel end-termination resistors (commonly 50Ω) to V_{TT} = ($V_{CCO}/2$) are typically placed on the board close to any receiver. Depending on the board topology, source-termination series resistors help match the output driver impedance to the transmission line and end-termination impedances, to reduce reflections and improve signal integrity. Optional on-die untuned input split termination feature (ODT) provides thevenin equivalent resistance of 2R (where R = Z_0) to the $V_{CCO}/2$. The differential (DIFF_) versions use complementary single-ended drivers for outputs, and differential receivers for inputs.

SSTL15, SSTL135, SSTL12, DIFF_SSTL15, DIFF_SSTL135, DIFF_SSTL12

Table 1-41: **Available I/O Bank Type**

HR	HP
Available	Available

Parallel end-termination resistors (commonly 50Ω) to V_{TT} = (V_{CCO}/2) are typically placed on the board close to any receiver. Depending on the board topology, source-termination series resistors help match the output driver impedance to the transmission line and end-termination impedances, to reduce reflections and improve signal integrity. Optional on-die untuned input split termination feature (ODT) provides thevenin equivalent resistance of 2R (where R = Z_0) to the V_{CCO}/2. Untuned on-die source termination feature (OUTPUT_IMPEDANCE) provides the option of 40Ω, 48Ω, or 60Ω of driver impedance in HP I/O banks. The driver output impedance is set to a default of 40Ω. The differential (DIFF_) versions use complementary single-ended drivers for outputs, and differential receivers for inputs.

SSTL15_DCI, SSTL135_DCI, SSTL12_DCI, DIFF_SSTL15_DCI, DIFF_SSTL135_DCI, DIFF_SSTL12_DCI

Table 1-42: **Available I/O Bank Type**

HR	HP
N/A	Available

The DCI standards provide tuned internal parallel split-termination resistors that are always present at the receivers. The value of both the resistance set by the ODT attributes, creates the Thevenin equivalent of 2R (where R = Z_0) to the V_{CCO}/2 mid-point level. The source termination feature (OUTPUT_IMPEDANCE) provides the option of 40Ω, 48Ω, or 60Ω tuned driver impedance in HP I/O banks. The driver output impedance is set to a default of 40Ω. The differential (DIFF_) versions use complementary single-ended drivers for outputs, and differential receivers for inputs.

SSTL18, SSTL15, SSTL135, SSTL12

Figure 1-62 shows a sample circuit illustrating a unidirectional termination technique for SSTL18, SSTL15, SSTL135, or SSTL12. In a specific circuit, all drivers and receivers must be at the same voltage level (1.8V, 1.5V, 1.35V, or 1.2V); they are not interchangeable.

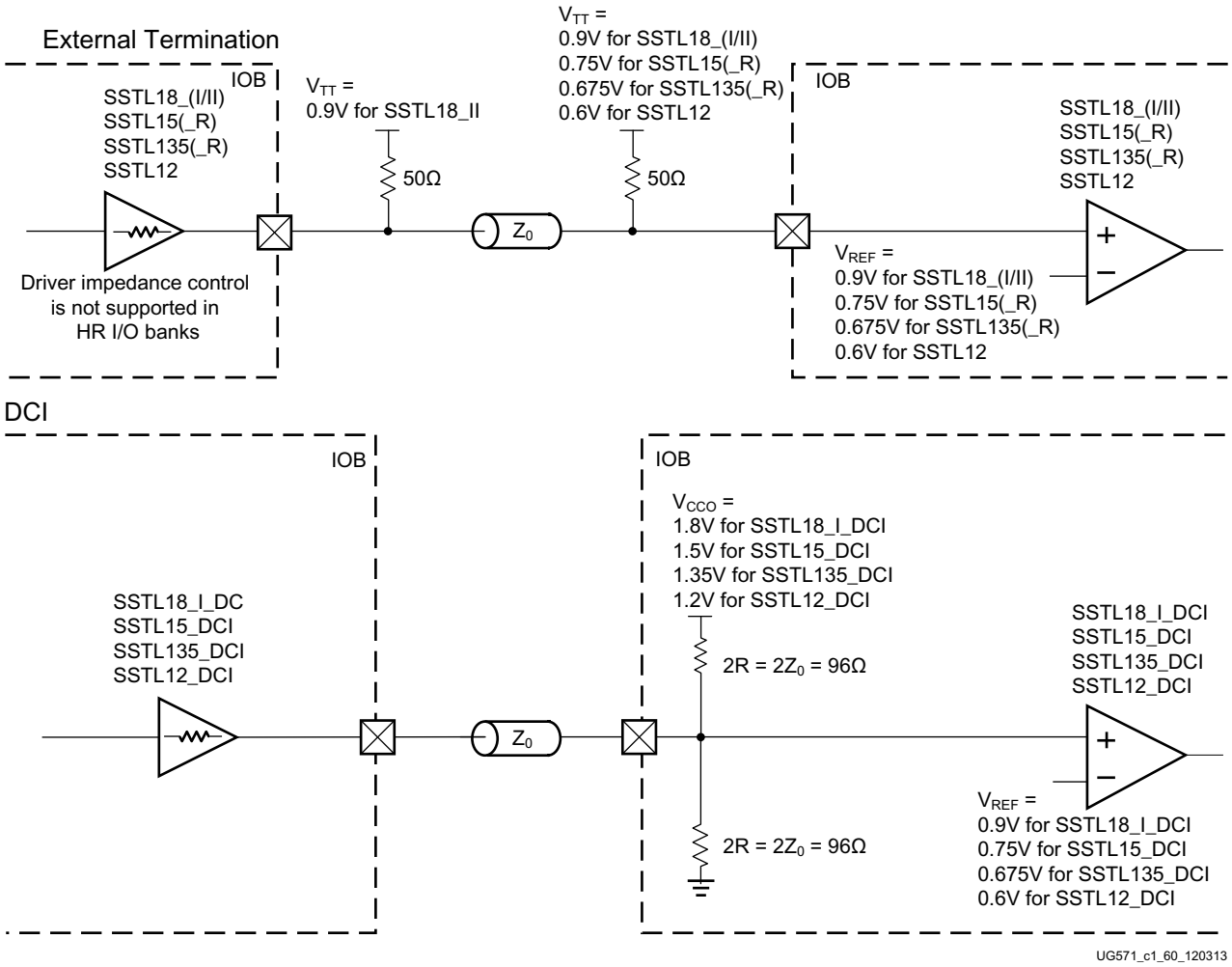

Figure 1-62: **SSTL18, SSTL15, SSTL135, or SSTL12 Unidirectional Termination**

Figure 1-63 shows a sample circuit illustrating a bidirectional termination technique for SSTL18, SSTL15, SSTL135, or SSTL12. In a specific circuit, all drivers and receivers must be at the same voltage level (1.8V, 1.5V, 1.35V, or 1.2V); they are not interchangeable.

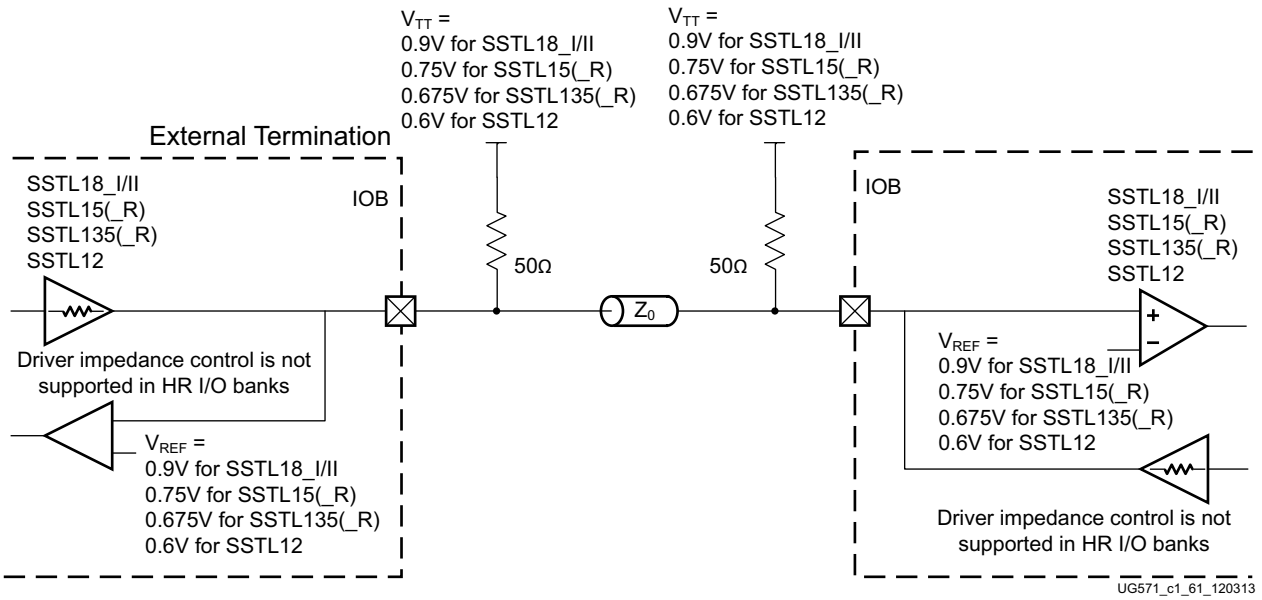

Figure 1-63: **SSTL18, SSTL15, SSTL135, or SSTL12 Bidirectional Termination**

Figure 1-64 shows a sample circuit illustrating a bidirectional termination technique for SSTL18, SSTL15, SSTL135, or SSTL12 with DCI. In a specific circuit, all drivers and receivers must be at the same voltage level (1.8V, 1.5V, 1.35V, or 1.2V); they are not interchangeable. DCI standards are only supported in HP I/O banks.

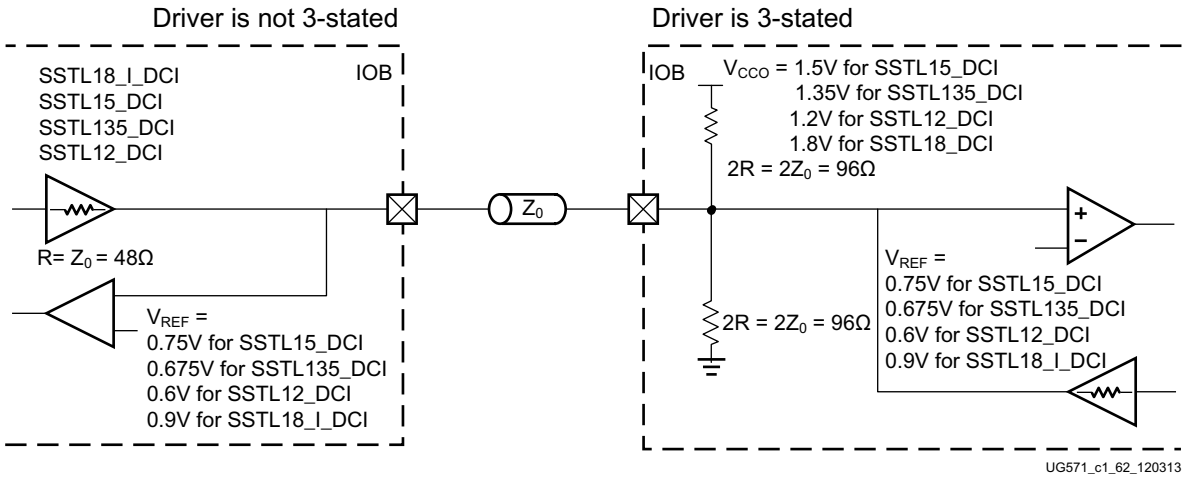

Figure 1-64: **SSTL18_DCI, SSTL15_DCI, SSTL135_DCI, or SSTL12_DCI Bidirectional Termination**

Differential SSTL18, SSTL15, SSTL135, SSTL12

Figure 1-65 shows a sample circuit illustrating a termination technique for differential SSTL18, SSTL15, SSTL135, or SSTL12 with unidirectional termination. In a specific circuit, all drivers and receivers must be at the same voltage level (1.8V, 1.5V, 1.35V, or 1.2V); they are not interchangeable.

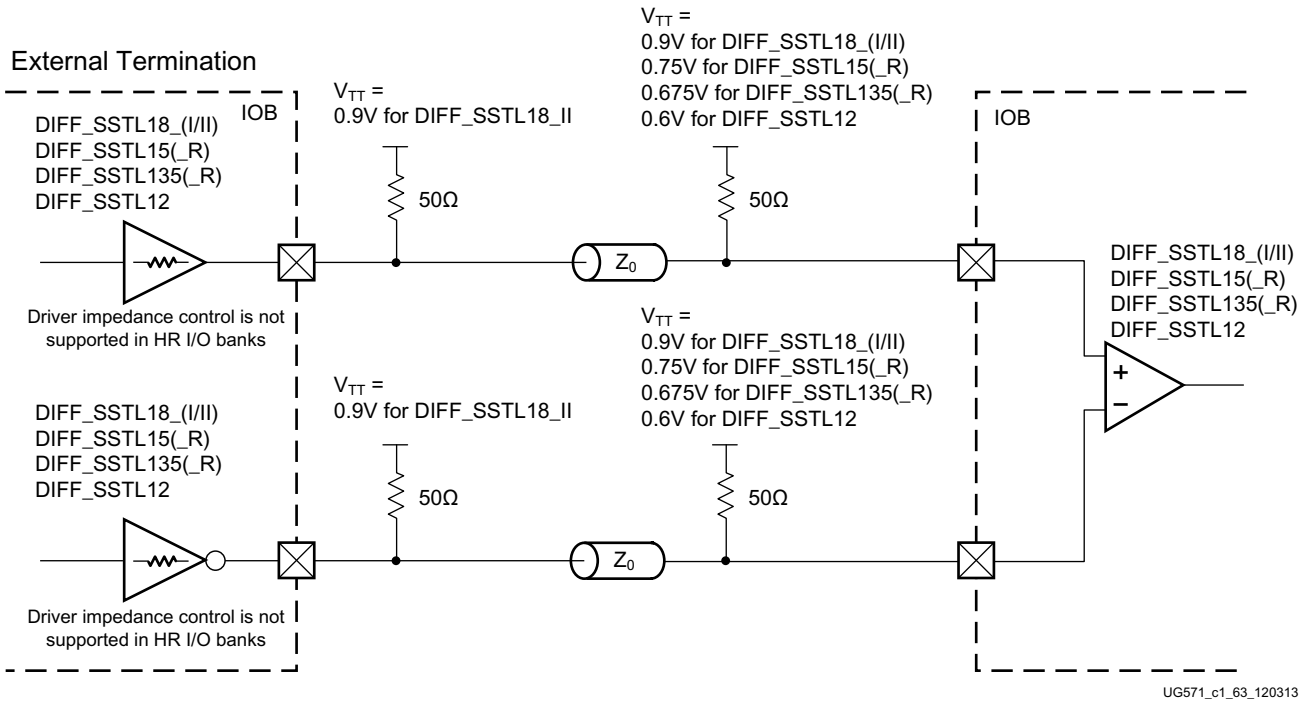

Figure 1-65: **Differential SSTL18, SSTL15, SSTL135, or SSTL12 Unidirectional Termination**

Figure 1-66 shows a sample circuit illustrating a termination technique for differential SSTL18, SSTL15, SSTL135, or SSTL12 with unidirectional DCI termination. In a specific circuit, all drivers and receivers must be at the same voltage level (1.8V, 1.5V, 1.35V, or 1.2V); they are not interchangeable.

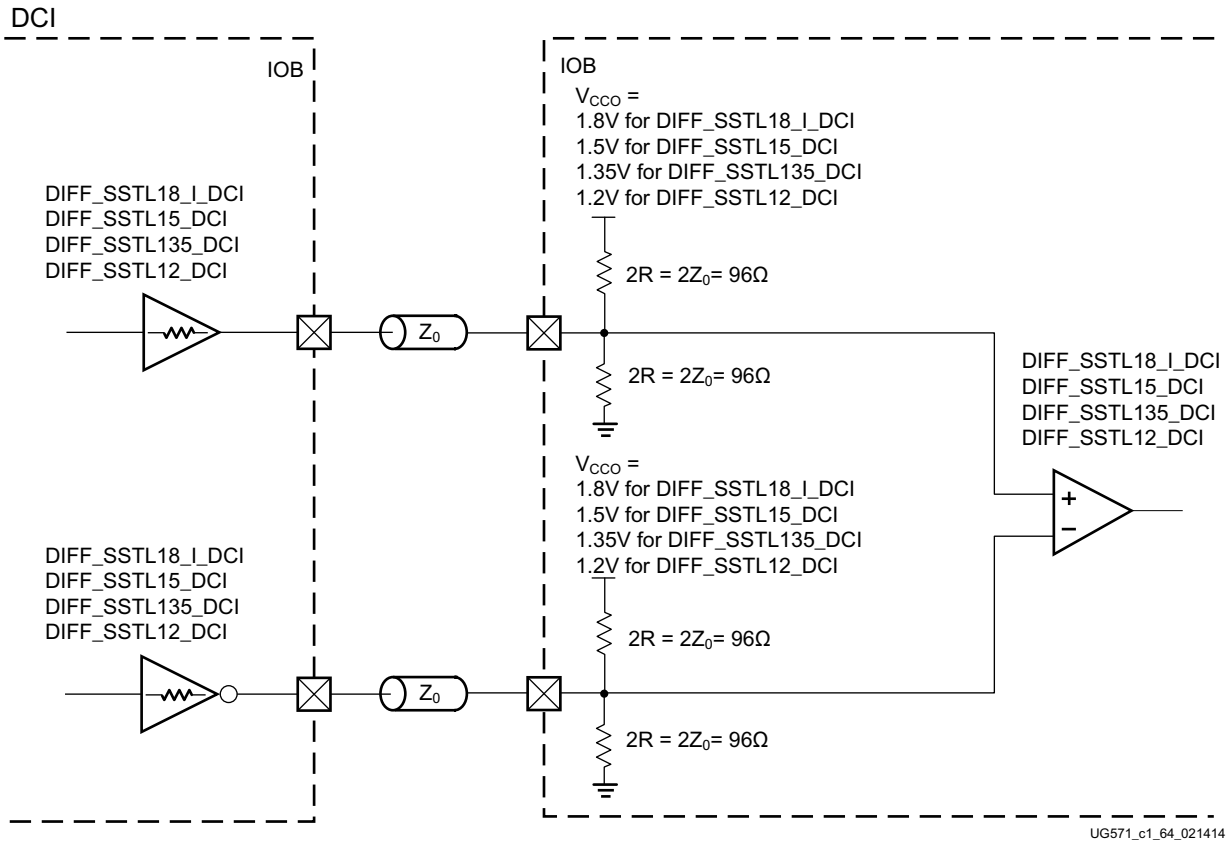

Figure 1-66: **Differential SSTL18, SSTL15, SSTL135, or SSTL12 Unidirectional DCI Termination**

Figure 1-67 shows a sample circuit illustrating a termination technique for differential SSTL18, SSTL15, SSTL135, or SSTL12 with bidirectional termination. In a specific circuit, all drivers and receivers must be at the same voltage level (1.8V, 1.5V, 1.35V, or 1.2V); they are not interchangeable.

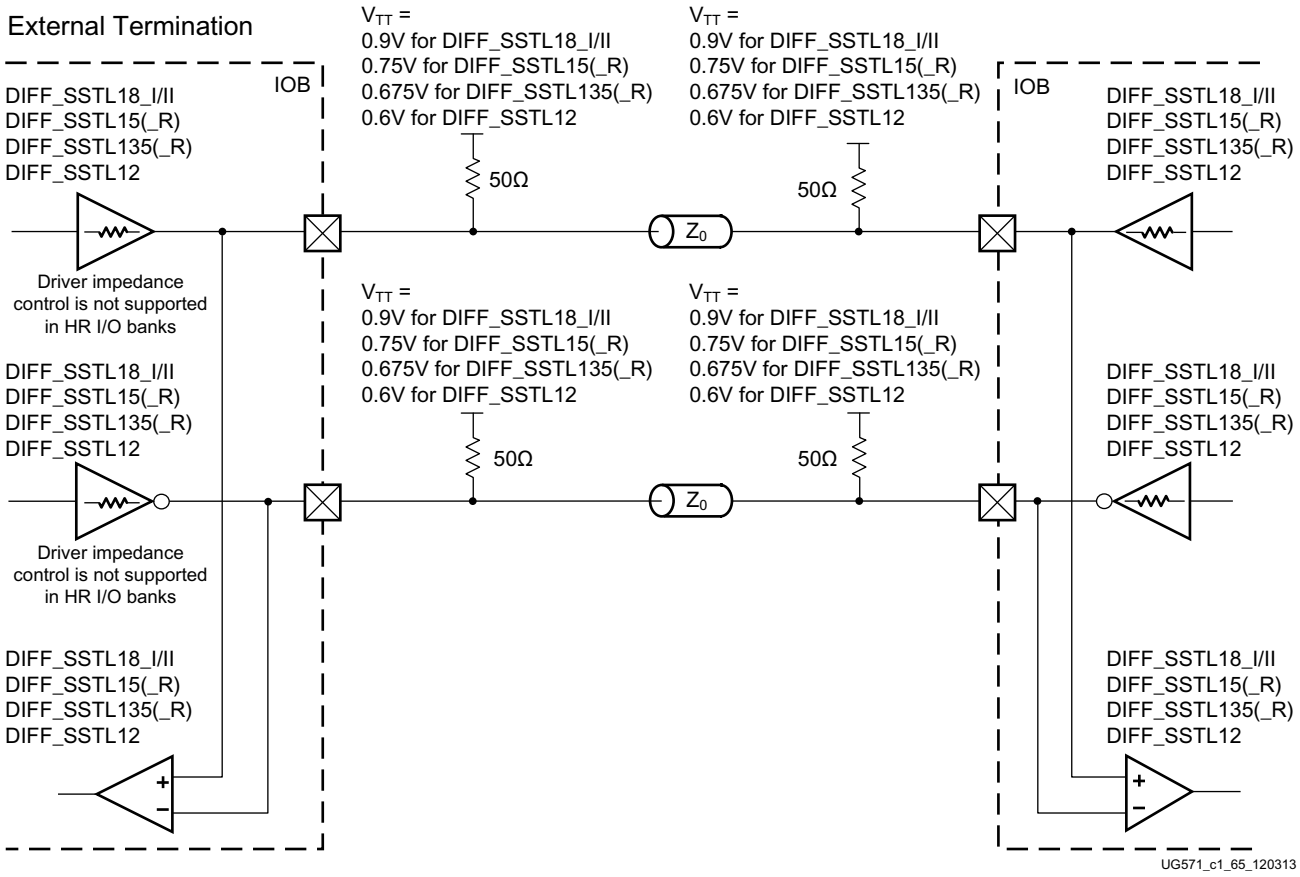

Figure 1-67: **Differential SSTL18, SSTL15, SSTL135, or SSTL12 with Bidirectional Termination**

Figure 1-68 shows a sample circuit illustrating a termination technique for differential SSTL18, SSTL15, SSTL135, or SSTL12 with bidirectional DCI termination. In a specific circuit, all drivers and receivers must be at the same voltage level (1.8V, 1.5V, 1.35V, or 1.2V); they are not interchangeable. DCI standards are supported only in HP I/Os.

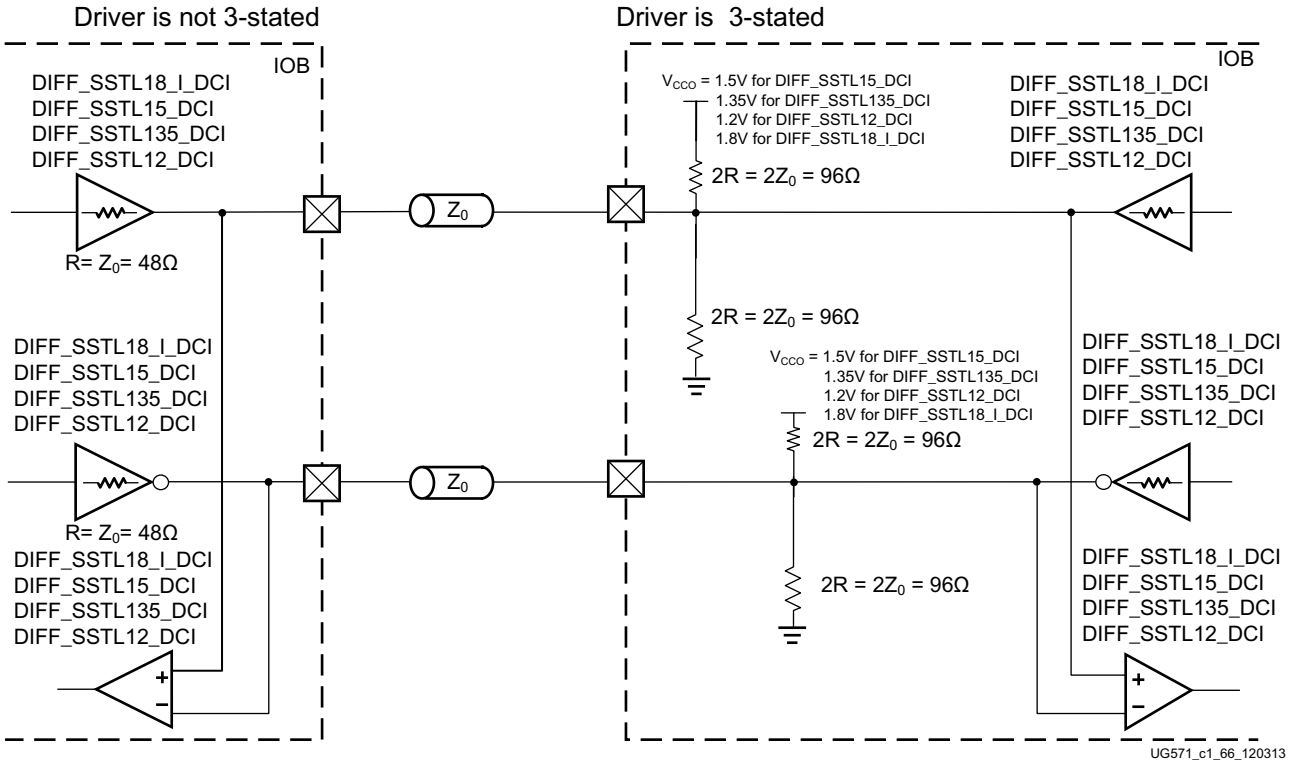

Figure 1-68: **Differential SSTL18, SSTL15, SSTL135, or SSTL12 with Bidirectional DCI Termination**

Table 1-43 lists the allowed attributes for SSTL I/O standards.

Table 1-43: **SSTL Allowed Attributes**

Attributes	IBUF/IBUFE3/IBUFDS/IBUFDSE3				OBUF/OBUFT				IOBUF/IOBUFE3/IOBUFDS/IOBUFDSE3			
	HP I/O		HR I/O		HP I/O		HR I/O		HP I/O		HR I/O	
	Allowed Values	Default	Allowed Values	Default	Allowed Values	Default	Allowed Values	Default	Allowed Values	Default	Allowed Values	Default
IOSTANDARD	SSTL12 SSTL135 SSTL15 SSTL18_I		SSTL12 SSTL135 SSTL135_R SSTL15 SSTL15_R SSTL18_I		SSTL12 SSTL135 SSTL15 SSTL18_I		SSTL12 SSTL135 SSTL135_R SSTL15 SSTL15_R SSTL18_I		SSTL12 SSTL135 SSTL15 SSTL18_I		SSTL12 SSTL135 SSTL135_R SSTL15 SSTL15_R SSTL18_I	
SLEW	N/A		N/A		FAST, MEDIUM, SLOW	SLOW	FAST SLOW	SLOW	FAST, MEDIUM, SLOW	SLOW	FAST SLOW	SLOW
ODT	RTT_40 RTT_48 RTT_60 RTT_NONE	RTT_NONE	RTT_40 RTT_48 RTT_60 RTT_NONE	RTT_NONE	N/A		N/A		RTT_40 RTT_48 RTT_60 RTT_NONE(1)	RTT_NONE	RTT_40 RTT_48 RTT_60 RTT_NONE	RTT_NONE
OUTPUT_ IMPEDANCE	N/A		N/A		RDRV_40_40 RDRV_48_48 RDRV_60_60	RDRV_40_40	N/A		RDRV_40_40 RDRV_48_48 RDRV_60_60(1)	RDRV_40_40	N/A	

Table 1-43: **SSTL Allowed Attributes *(Cont'd)***

Attributes	IBUF/IBUFE3/IBUFDS/IBUFDSE3				OBUF/OBUFT				IOBUF/IOBUFE3/IOBUFDS/IOBUFDSE3			
	HP I/O		HR I/O		HP I/O		HR I/O		HP I/O		HR I/O	
	Allowed Values	Default	Allowed Values	Default	Allowed Values	Default	Allowed Values	Default	Allowed Values	Default	Allowed Values	Default
IOSTANDARD	SSTL12_DCI SSTL135_DCI SSTL15_DCI SSTL18_I_DCI		N/A		SSTL12_DCI SSTL135_DCI SSTL15_DCI SSTL18_I_DCI		N/A		SSTL12_DCI SSTL135_DCI SSTL15_DCI SSTL18_I_DCI		N/A	
SLEW	N/A		N/A		FAST, MEDIUM, SLOW	SLOW	N/A		FAST, MEDIUM, SLOW	SLOW	N/A	
ODT	RTT_40 RTT_48 RTT_60	RTT_40	N/A		N/A		N/A		RTT_40 RTT_48 RTT_60[1][2]	RTT_40	N/A	
OUTPUT_ IMPEDANCE	N/A		N/A		RDRV_40_40 RDRV_48_48 RDRV_60_60	RDRV_40_40	N/A		RDRV_40_40 RDRV_48_48 RDRV_60_60[1]	RDRV_40_40	N/A	
IOSTANDARD	DIFF_SSTL12 DIFF_SSTL135 DIFF_SSTL15 DIFF_SSTL18_I		DIFF_SSTL12 DIFF_SSTL135 DIFF_SSTL15 DIFF_SSTL18_I		DIFF_SSTL12 DIFF_SSTL135 DIFF_SSTL15 DIFF_SSTL18_I		DIFF_SSTL12 DIFF_SSTL135 DIFF_SSTL15 DIFF_SSTL18_I		DIFF_SSTL12 DIFF_SSTL135 DIFF_SSTL15 DIFF_SSTL18_I		DIFF_SSTL12 DIFF_SSTL135 DIFF_SSTL15 DIFF_SSTL18_I	
SLEW	N/A		N/A		FAST MEDIUM SLOW	SLOW	FAST SLOW	SLOW	FAST MEDIUM SLOW	SLOW	FAST SLOW	SLOW
DQS_BIAS	TRUE FALSE	FALSE	TRUE FALSE	FALSE	N/A		N/A		TRUE FALSE	FALSE	TRUE FALSE	FALSE
ODT	RTT_40 RTT_48 RTT_60 RTT_NONE	RTT_NONE	RTT_40 RTT_48 RTT_60 RTT_NONE	RTT_NONE	N/A		N/A		RTT_40 RTT_48 RTT_60 RTT_NONE[1]	RTT_NONE	RTT_40 RTT_48 RTT_60 RTT_NONE	RTT_NONE
OUTPUT_ IMPEDANCE	N/A		N/A		RDRV_40_40 RDRV_48_48 RDRV_60_60	RDRV_40_40	N/A		RDRV_40_40 RDRV_48_48 RDRV_60_60[1]	RDRV_40_40	N/A	

Table 1-43: **SSTL Allowed Attributes *(Cont'd)***

Attributes	IBUF/IBUFE3/IBUFDS/IBUFDSE3				OBUF/OBUFT				IOBUF/IOBUFE3/IOBUFDS/IOBUFDSE3			
	HP I/O		HR I/O		HP I/O		HR I/O		HP I/O		HR I/O	
	Allowed Values	Default	Allowed Values	Default	Allowed Values	Default	Allowed Values	Default	Allowed Values	Default	Allowed Values	Default
IOSTANDARD	DIFF_SSTL12_DCI DIFF_SSTL135_DCI DIFF_SSTL15_DCI DIFF_SSTL18_I_DCI		N/A		DIFF_SSTL12_DCI DIFF_SSTL135_DCI DIFF_SSTL15_DCI DIFF_SSTL18_I_DCI		N/A		DIFF_SSTL12_DCI DIFF_SSTL135_DCI DIFF_SSTL15_DCI DIFF_SSTL18_I_DCI		N/A	
SLEW	N/A		N/A		FAST MEDIUM SLOW	SLOW	N/A		FAST MEDIUM SLOW	SLOW	N/A	
DQS_BIAS	TRUE FALSE	FALSE	N/A		N/A		N/A		TRUE FALSE	FALSE	N/A	
ODT	RTT_40 RTT_48 RTT_60(2)	RTT_40	N/A		N/A		N/A		RTT_40 RTT_48 RTT_60(1)(2)	RTT_40	N/A	
OUTPUT_ IMPEDANCE	N/A		N/A		RDRV_40_40 RDRV_48_48 RDRV_60_60	RDRV_40_40	N/A		RDRV_40_40 RDRV_48_48 RDRV_60_60(1)	RDRV_40_40	N/A	
IOSTANDARD	N/A		DIFF_SSTL135_R DIFF_SSTL15_R		N/A		DIFF_SSTL135_R DIFF_SSTL15_R		N/A		DIFF_SSTL135_R DIFF_SSTL15_R	
SLEW	N/A		N/A		N/A		FAST SLOW	SLOW	N/A		FAST SLOW	SLOW
ODT	N/A		RTT_40 RTT_48 RTT_60 RTT_NONE	RTT_NONE	N/A		N/A		N/A		RTT_40 RTT_48 RTT_60 RTT_NONE	RTT_NONE

Notes:

1. The allowed bidirectional configuration combinations for driver output impedance (OUTPUT_IMPEDANCE) and ODT are listed in Table 1-36.
2. ODT = RTT_NONE is not a valid setting for DCI I/O standards.

Table 1-44 lists the allowed attributes for SSTL Class II I/O standards.

Table 1-44: **SSTL Class II Allowed Attributes**

Attributes	IBUF/IBUFDS			OBUF/OBUFT			IOBUF/IOBUFDS		
	HP I/O	HR I/O		HP I/O	HR I/O		HP I/O	HR I/O	
		Allowed Values	Default		Allowed Values	Default		Allowed Values	Default
IOSTANDARD	N/A	SSTL18_II DIFF_SSTL18_II		N/A	SSTL18_II DIFF_SSTL18_II		N/A	SSTL18_II DIFF_SSTL18_II	
SLEW	N/A	N/A		N/A	FAST SLOW	SLOW	N/A	FAST SLOW	SLOW
ODT	N/A	RTT_40 RTT_48 RTT_60 RTT_NONE	RTT_NONE	N/A	N/A		N/A	RTT_40 RTT_48 RTT_60 RTT_NONE	RTT_NONE

HSUL_12 (High Speed Unterminated Logic)

The HSUL_12 standard is for LPDDR2 and LPDDR3 memory buses. HSUL_12 is defined by the JEDEC standard JESD8-22 [Ref 8]. UltraScale devices support this standard for single-ended signaling and differential signaling. Similar to SSTL, this standard also requires a differential amplifier input buffer and a push-pull output buffer.

HSUL_12 and DIFF_HSUL_12

Table 1-45: **Available I/O Bank Type**

HR	HP
Available	Available

The differential (DIFF_) version uses complementary single-ended drivers for outputs, and differential receivers for inputs. In HP I/O banks, an optional on-die untuned input single termination feature (ODT) provides a weak pull-up to V_{CCO}. The untuned on-die source termination feature (OUTPUT_IMPEDANCE) provides the option of 40Ω, 48Ω, or 60Ω of driver impedance in HP I/O banks. The driver output impedance is set to a default of 48Ω.

HSUL_DCI_12 and DIFF_HSUL_12_DCI

Table 1-46: **Available I/O Bank Type**

HR	HP
N/A	Available

DCI provides a tuned on-die input single termination to V_{CCO} on the receivers and a tuned on-die source termination option (OUTPUT_IMPEDANCE) of 40Ω, 48Ω, or 60Ω of driver impedance in HP I/O banks. The impedances are scaled from the reference resistor on the VRP pin. The driver output impedance is set to a default of 48Ω. The differential (DIFF_) versions use complementary single-ended drivers for outputs, and differential receivers for inputs.

HSUL_12

Figure 1-69 shows a sample circuit illustrating a unidirectional board topology for HSUL_12. Only HP I/O banks support the DCI version.

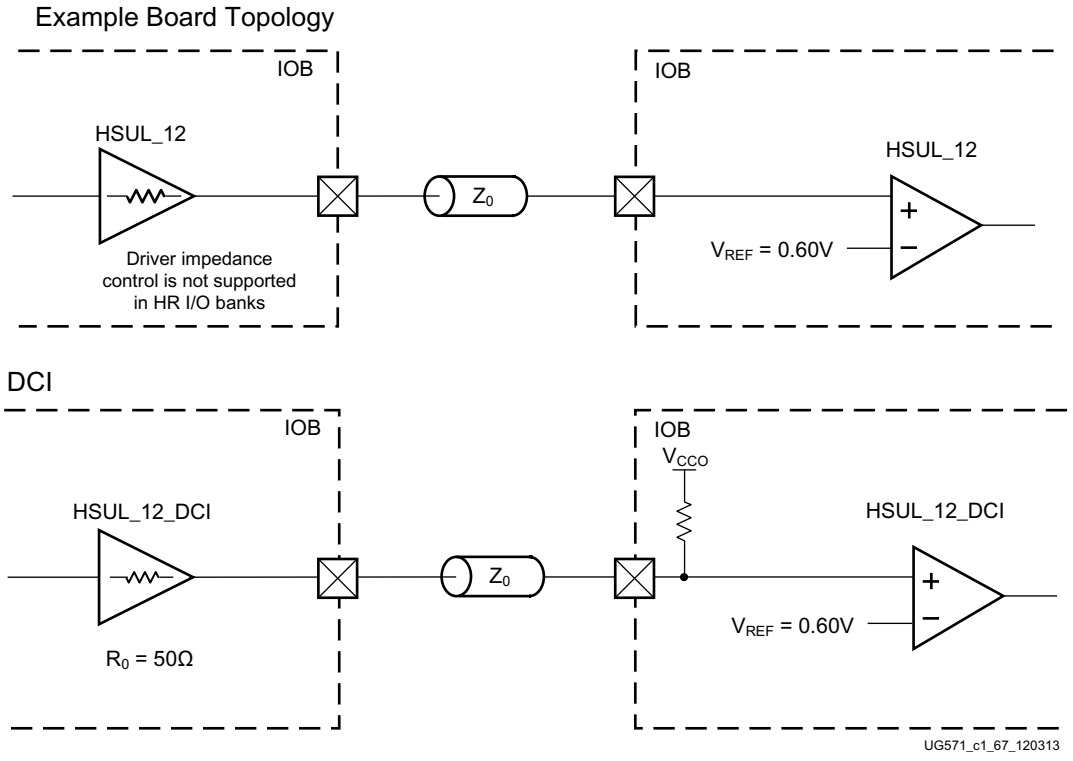

Figure 1-69: **HSUL_12 with Unidirectional Signaling**

Figure 1-70 shows a sample circuit illustrating a bidirectional board topology (with no termination) for HSUL_12. Only HP I/O banks support the DCI version.

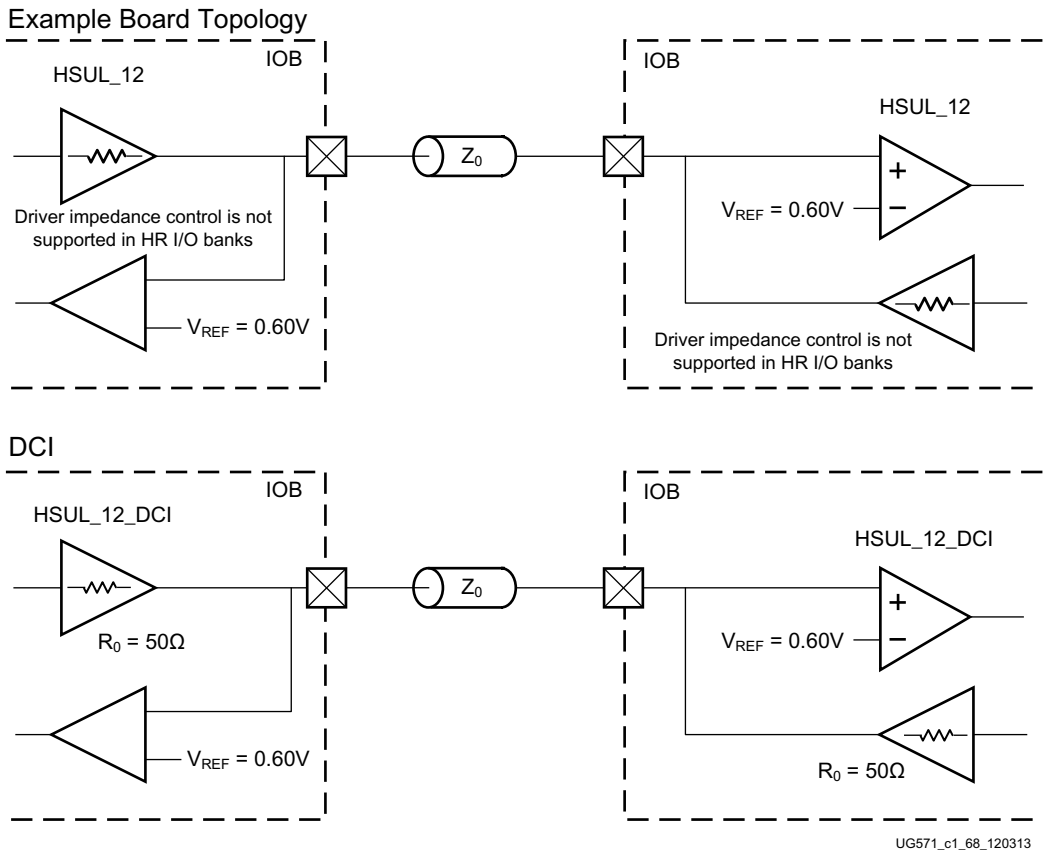

Figure 1-70: **HSUL_12 with Bidirectional Signaling**

Differential HSUL_12

Figure 1-71 shows a sample circuit illustrating a board topology for differential HSUL_12 with unidirectional signaling.

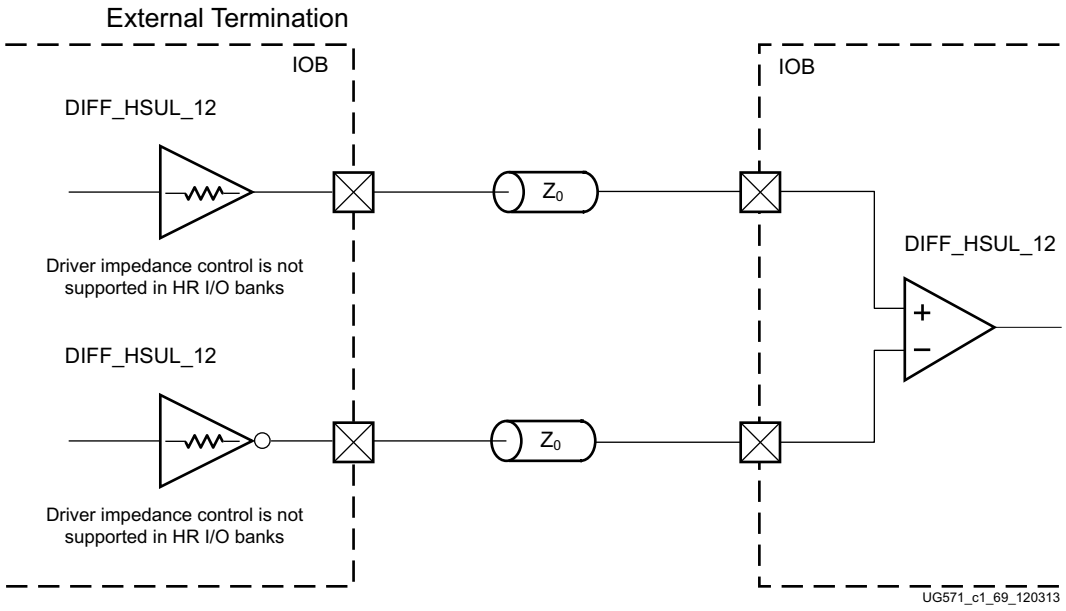

Figure 1-71: **Differential HSUL_12 with Unidirectional Signaling**

Figure 1-72 shows a sample circuit illustrating a board topology for differential HSUL_12 with unidirectional DCI signaling.

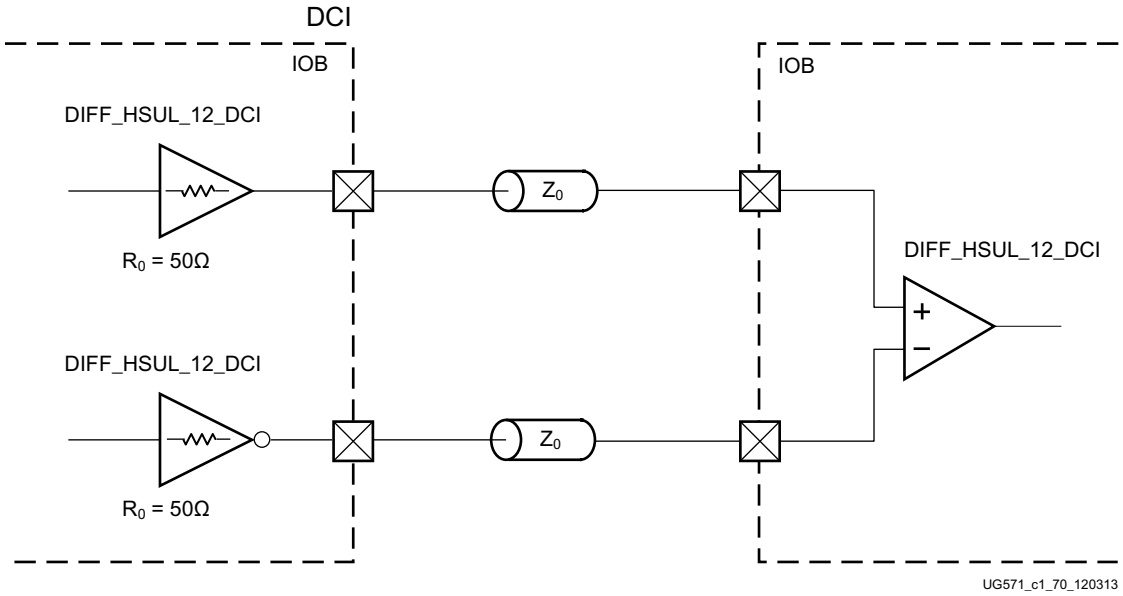

Figure 1-72: **Differential HSUL_12 with Unidirectional DCI Signaling**

Figure 1-73 shows a sample circuit illustrating a board topology for differential HSUL_12 with bidirectional signaling.

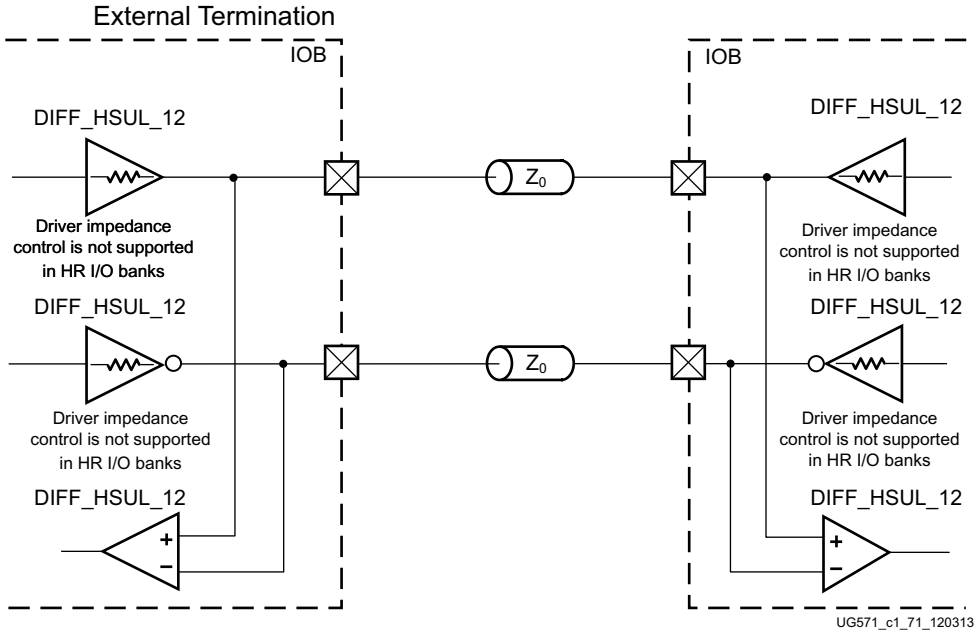

Figure 1-73: **Differential HSUL_12 with Bidirectional Signaling**

Figure 1-74 shows a sample circuit illustrating a board topology for differential HSUL_12 with bidirectional DCI signaling.

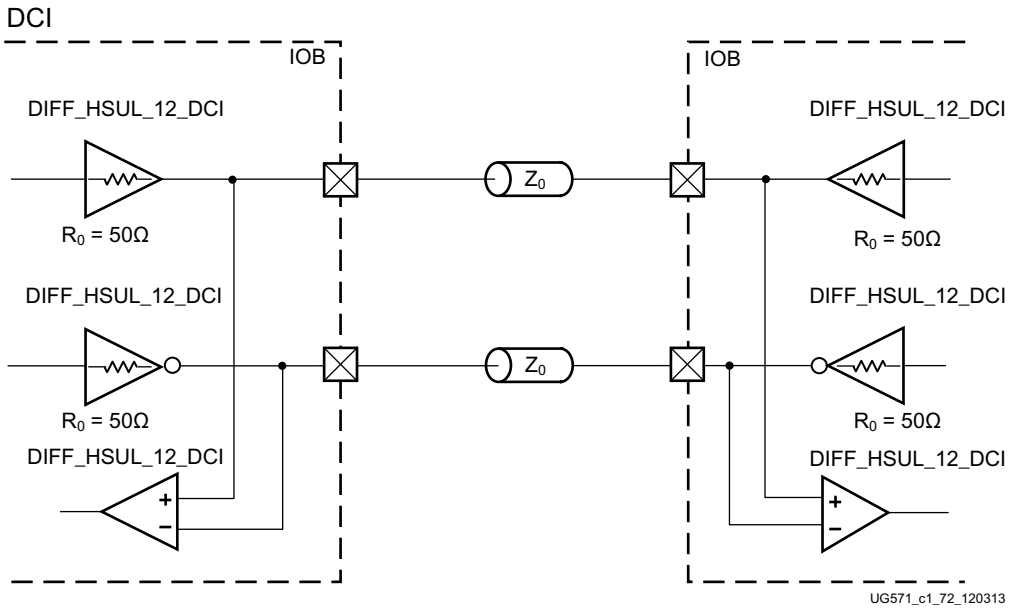

Figure 1-74: **Differential HSUL_12 with DCI Bidirectional Signaling**

Table 1-47 lists the allowed attributes for HSUL I/O standards.

Table 1-47: **HSUL Allowed Attributes**

Attributes	IBUF/IBUFE3/IBUFDS/IBUFDSE3				OBUF/OBUFT				IOBUF/IOBUFE3/IOBUFDS/IOBUFDSE3			
	HP I/O		HR I/O		HP I/O		HR I/O		HP I/O		HR I/O	
	Allowed Values	Default	Allowed Values	Default	Allowed Values	Default	Allowed Values	Default	Allowed Values	Default	Allowed Values	Default
IOSTANDARD	HSUL_12 DIFF_HSUL_12		HSUL_12 DIFF_HSUL_12		HSUL_12 DIFF_HSUL_12		HSUL_12 DIFF_HSUL_12		HSUL_12 DIFF_HSUL_12		HSUL_12 DIFF_HSUL_12	
SLEW	N/A		N/A		FAST MEDIUM SLOW	SLOW	FAST SLOW	SLOW	FAST MEDIUM SLOW	SLOW	FAST SLOW	SLOW
ODT	RTT_120 RTT_240 RTT_NONE	RTT_NONE	N/A		N/A		N/A		RTT_120 RTT_240 RTT_NONE	RTT_NONE	N/A	
OUTPUT_ IMPEDANCE	N/A		N/A		RDRV_40_40 RDRV_48_48 RDRV_60_60	RDRV_48_48	N/A		RDRV_40_40 RDRV_48_48 RDRV_60_60	RDRV_48_48	N/A	
IOSTANDARD	HSUL_12_DCI DIFF_HSUL_12_DCI		N/A		HSUL_12_DCI DIFF_HSUL_12_DCI		N/A		HSUL_12_DCI DIFF_HSUL_12_DCI		N/A	
SLEW	N/A		N/A		FAST MEDIUM SLOW	SLOW	N/A		FAST MEDIUM SLOW	SLOW	N/A	
ODT	RTT_120 RTT_240 RTT_NONE	RTT_NONE	N/A		N/A		N/A		RTT_120 RTT_240 RTT_NONE	RTT_NONE	N/A	

POD12 and POD10 (Pseudo Open Drain)

Pseudo Open Drain (POD) standards POD12 and POD10 are intended for DDR4, DDR4L, and LLDRAM3 applications. POD12 and POD10 are only available in HP I/O banks and use V_{REF}.

POD10, POD12, DIFF_POD10, and DIFF_POD12

Table 1-48: **Available I/O Bank Type**

HR	HP
N/A	Available

The differential (DIFF_) versions (DIFF_POD10 and DIFF_POD12) use complementary single-ended drivers for outputs, and differential receivers for inputs. Optional on-die untuned input single termination feature (ODT) provides pull-up to V_{CCO}. The untuned on-die source termination feature (OUTPUT_IMPEDANCE) provides the option of 40Ω, 48Ω, or 60Ω of driver impedance in HP I/O banks. The driver output impedance is set to a default of 40Ω. POD12 standards also have optional EQUALIZATION and OFFSET_CNTRL features in the receivers and PRE_EMPHASIS in the drivers.

POD10_DCI, POD12_DCI, DIFF_POD10_DCI, and DIFF_POD12_DCI

Table 1-49: **Available I/O Bank Type**

HR	HP
N/A	Available

DCI provides a tuned single termination to V_{CCO} at the receiver that matches the ODT attribute setting. The differential (DIFF_) versions use complementary single-ended drivers for outputs, and differential receivers for inputs.

DCI provides a tuned on-die single termination (ODT) pull-up to V_{CCO} in the receivers and a source termination option (OUTPUT_IMPEDANCE) of 40Ω, 48Ω, or 60Ω in the driver. The driver output impedance is set to a default of 40Ω. POD12 standards also have optional EQUALIZATION and OFFSET_CNTRL features in the receivers and PRE_EMPHASIS in the drivers.

POD

Figure 1-75 shows a sample circuit illustrating a unidirectional board topology for POD (1.0V or 1.2V) with matched driver and receiver termination values. Only HP I/O banks support these standards.

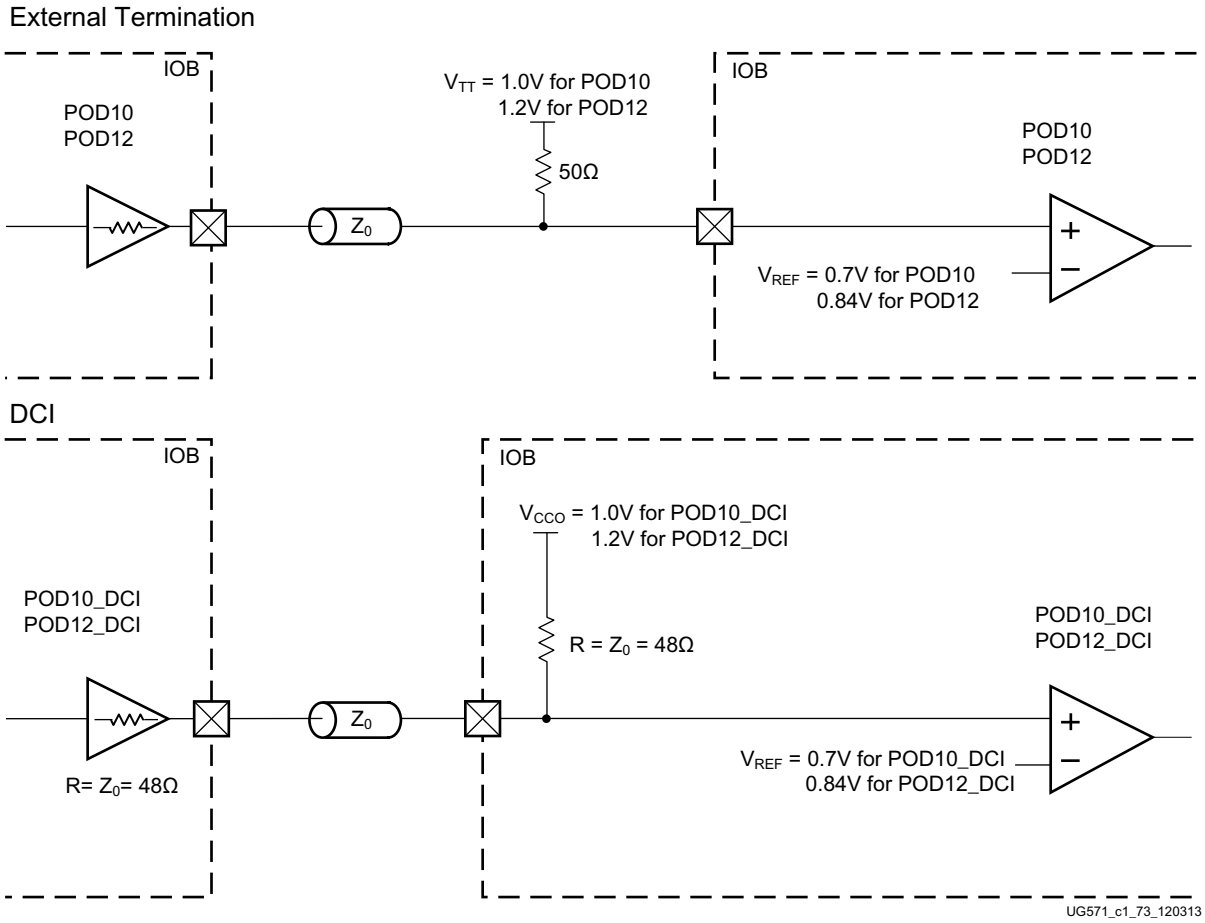

Figure 1-75: **POD with Unidirectional Signaling**

Figure 1-76 shows a sample circuit illustrating a termination technique for POD (1.0V or 1.2V) with bidirectional termination and with matched driver and receiver termination values. In a specific circuit, all drivers and receivers must be at the same voltage level (1.0V or 1.2V); they are not interchangeable.

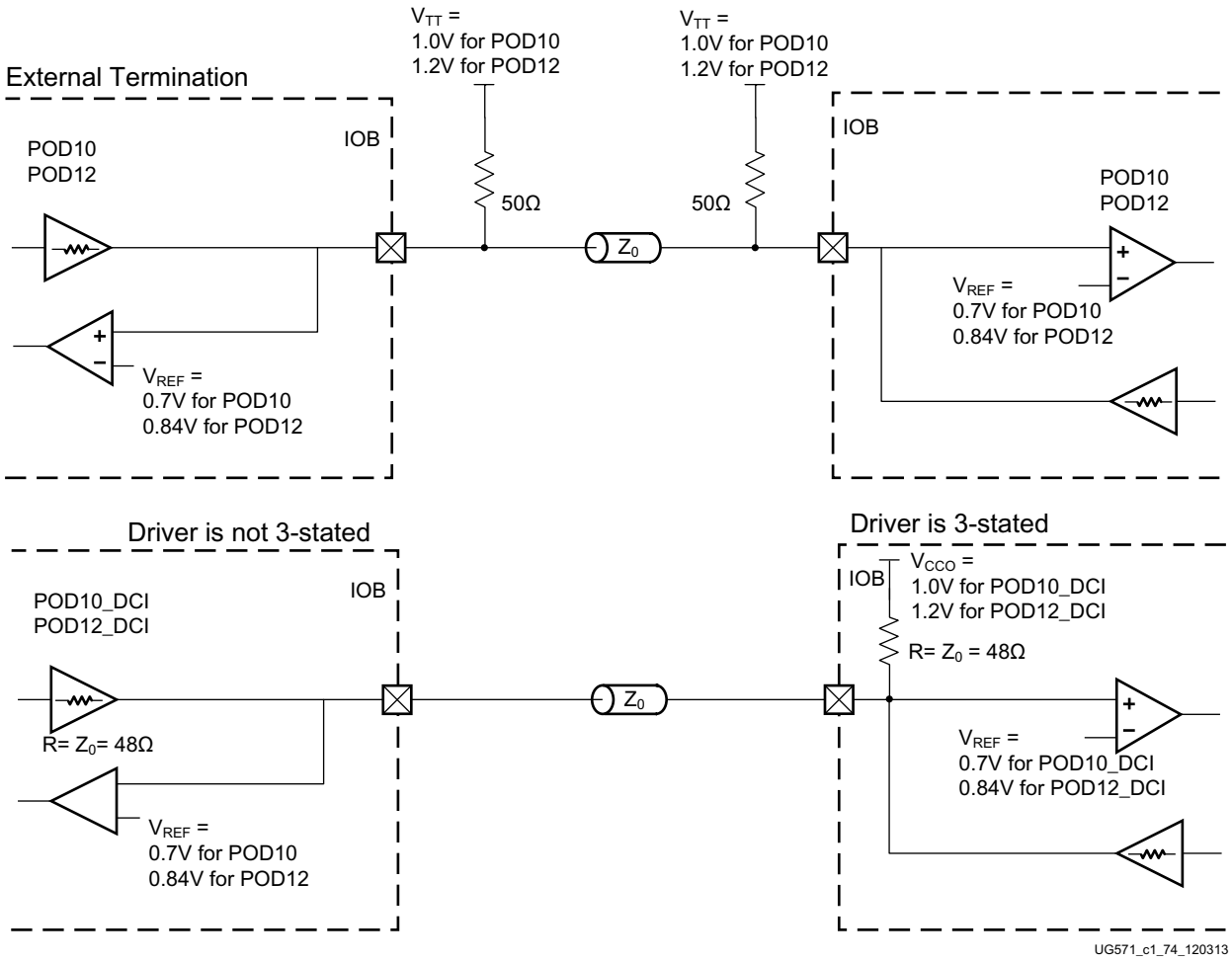

Figure 1-76: **POD with Bidirectional Signaling**

Differential POD

Figure 1-77 shows a sample circuit illustrating a termination technique for differential POD (1.0V, 1.2V) with unidirectional termination and with matched driver and receiver termination values. In a specific circuit, all drivers and receivers must be at the same voltage level (1.2V or 1.0V); they are not interchangeable.

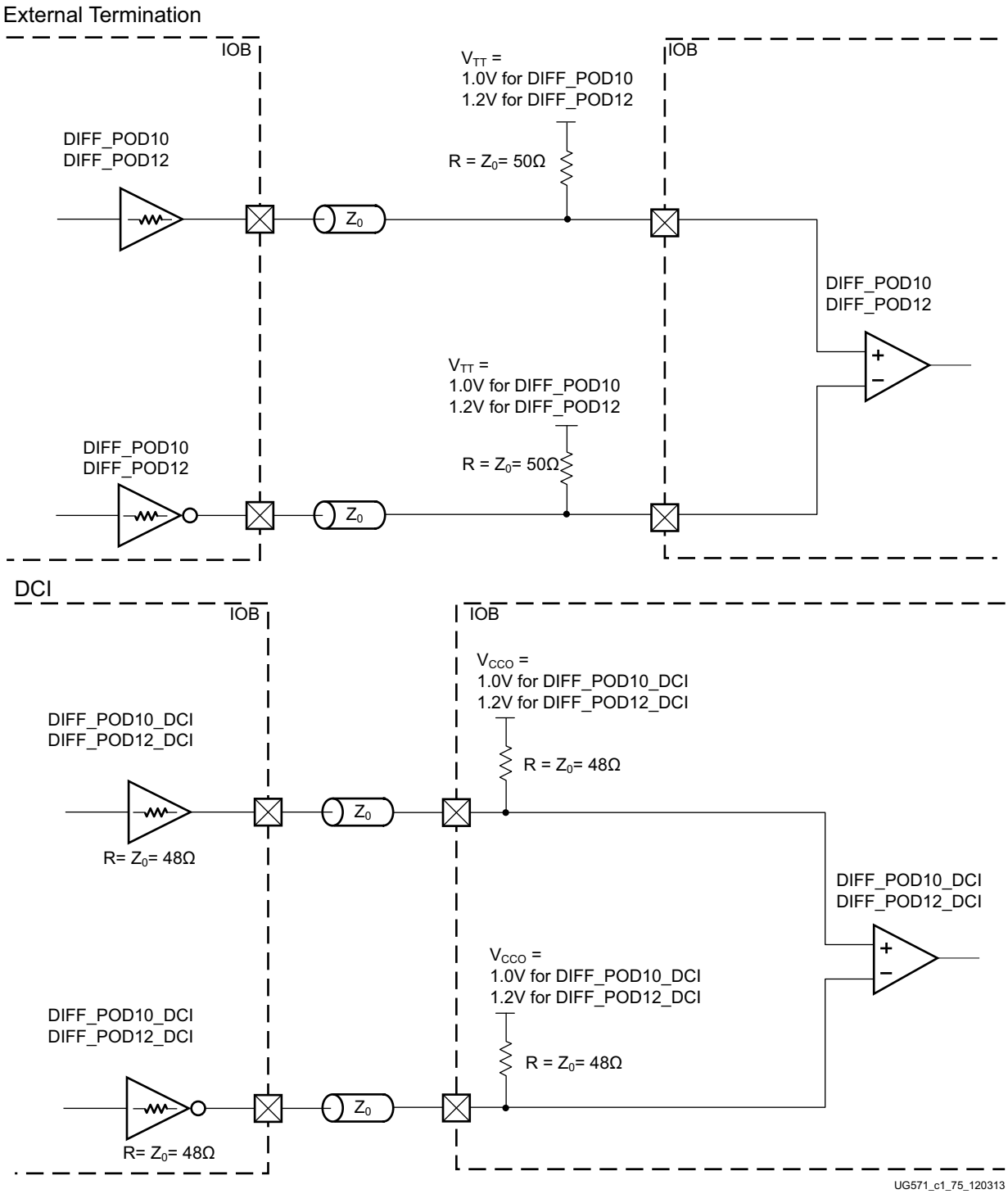

Figure 1-77: **Differential POD with Unidirectional Signaling**

Figure 1-78 shows a sample circuit illustrating a termination technique for differential POD (1.0V or 1.2V) with bidirectional termination and with matched driver and receiver termination values. In a specific circuit, all drivers and receivers must be at the same voltage level (1.0V or 1.2V); they are not interchangeable.

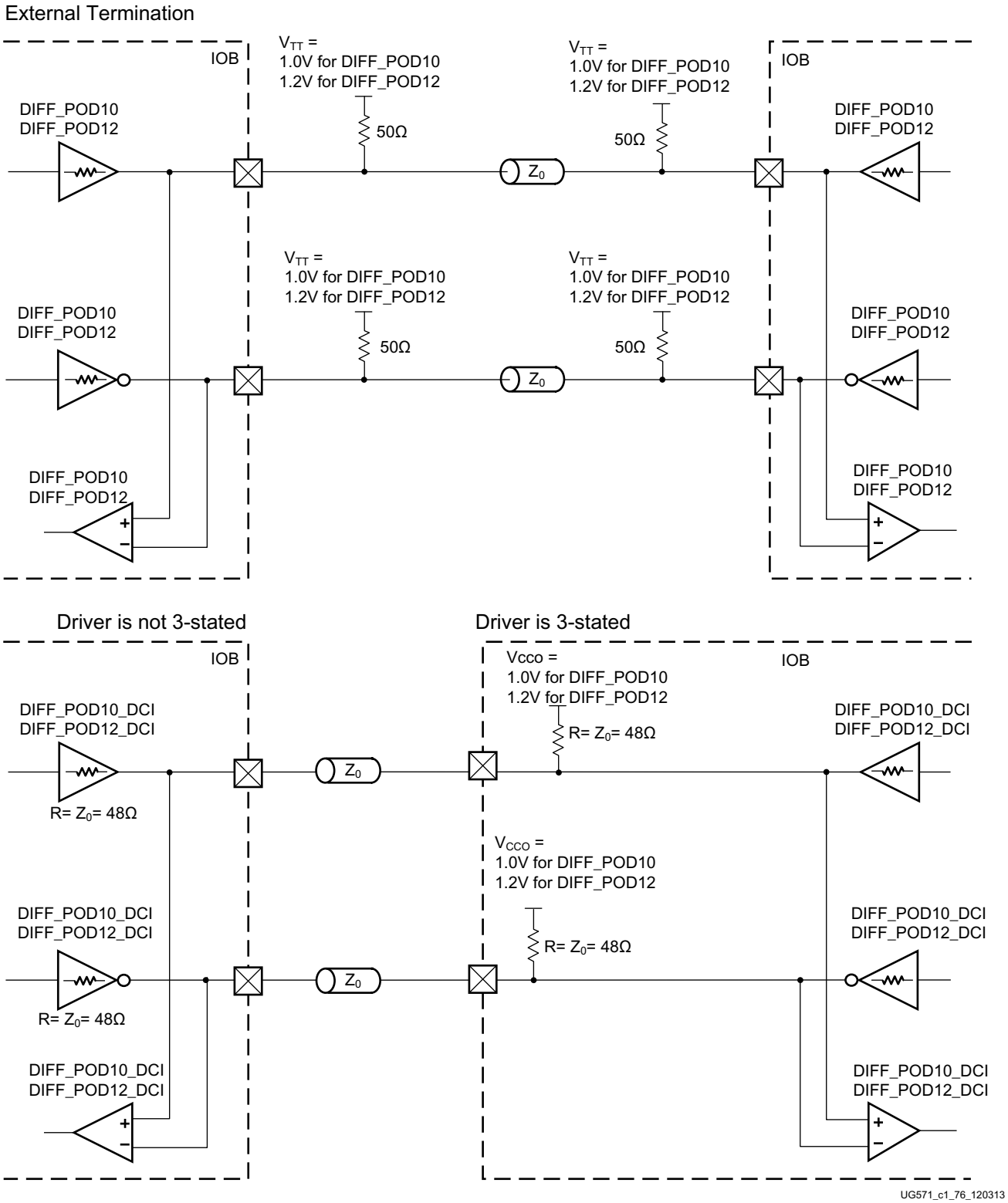

Figure 1-78: **Differential POD with Bidirectional Signaling**

Table 1-50 lists the allowed attributes for POD I/O standards.

Table 1-50: **POD Allowed Attributes**

Attributes	IBUF/IBUFE3/IBUFDS/IBUFDSE3			OBUF/OBUFT			IOBUF/IOBUFE3/IOBUFDS/IOBUFDSE3		
	HP I/O		HR I/O	HP I/O		HR I/O	HP I/O		HR I/O
	Allowed Values	Default		Allowed Values	Default		Allowed Values	Default	
IOSTANDARD	POD10 DIFF_POD10		N/A	POD10 DIFF_POD10		N/A	POD10 DIFF_POD10		N/A
SLEW	N/A		N/A	FAST MEDIUM SLOW	SLOW	N/A	FAST MEDIUM SLOW	SLOW	N/A
DQS_BIAS(5)	TRUE FALSE	FALSE	N/A	N/A		N/A	TRUE FALSE	FALSE	N/A
ODT	RTT_40, RTT_48 RTT_60, RTT_NONE	RTT_NONE	N/A	N/A		N/A	RTT_40, RTT_48 RTT_60, RTT_NONE(1)	RTT_NONE	N/A
OUTPUT_ IMPEDANCE	N/A		N/A	RDRV_40_40 RDRV_48_48 RDRV_60_60	RDRV_40_40	N/A	RDRV_40_40 RDRV_48_48 RDRV_60_60(1)	RDRV_40_40	N/A
IOSTANDARD	POD10_DCI DIFF_POD10_DCI		N/A	POD10_DCI DIFF_POD10_DCI		N/A	POD10_DCI DIFF_POD10_DCI		N/A
SLEW	N/A		N/A	FAST MEDIUM SLOW	SLOW	N/A	FAST MEDIUM SLOW	SLOW	N/A
DQS_BIAS(5)	TRUE FALSE	FALSE	N/A	N/A		N/A	TRUE FALSE	FALSE	N/A
ODT	RTT_40 RTT_48 RTT_60(2)	RTT_40	N/A	N/A		N/A	RTT_40 RTT_48 RTT_60(1)(2)	RTT_40	N/A
OUTPUT_ IMPEDANCE	N/A		N/A	RDRV_40_40 RDRV_48_48 RDRV_60_60	RDRV_40_40	N/A	RDRV_40_40 RDRV_48_48 RDRV_60_60(1)	RDRV_40_40	N/A

Table 1-50: **POD Allowed Attributes *(Cont'd)***

Attributes	IBUF/IBUFE3/IBUFDS/IBUFDSE3			OBUF/OBUFT			IOBUF/IOBUFE3/IOBUFDS/IOBUFDSE3		
	HP I/O		HR I/O	HP I/O		HR I/O	HP I/O		HR I/O
	Allowed Values	Default		Allowed Values	Default		Allowed Values	Default	
IOSTANDARD	POD12 DIFF_POD12		N/A	POD12 DIFF_POD12		N/A	POD12 DIFF_POD12		N/A
SLEW	N/A		N/A	FAST MEDIUM SLOW	SLOW	N/A	FAST MEDIUM SLOW	SLOW	N/A
PRE_EMPHASIS	N/A		N/A	RDRV_240 RDRV_NONE(4)	RDRV_NONE	N/A	RDRV_240 RDRV_NONE(3)	RDRV_NONE	N/A
EQUALIZATION	EQ_LEVEL0, EQ_LEVEL1, EQ_LEVEL2, EQ_LEVEL3, EQ_LEVEL4, EQ_NONE	EQ_NONE	N/A	N/A		N/A	EQ_LEVEL0, EQ_LEVEL1, EQ_LEVEL2, EQ_LEVEL3, EQ_LEVEL4, EQ_NONE	EQ_NONE	N/A
OFFSET_CNTRL	CNTRL_NONE FABRIC	CNTRL_NONE	N/A	N/A		N/A	CNTRL_NONE FABRIC	CNTRL_NONE	N/A
DQS_BIAS(5)	TRUE FALSE	FALSE	N/A	N/A		N/A	TRUE FALSE	FALSE	N/A
ODT	RTT_40 RTT_48 RTT_60 RTT_NONE	RTT_NONE	N/A	N/A		N/A	RTT_40 RTT_48 RTT_60 (RTT_NONE)(3)	RTT_NONE	N/A
OUTPUT_ IMPEDANCE	N/A		N/A	RDRV_40_40 RDRV_48_48 RDRV_60_60(4)	RDRV_40_40	N/A	RDRV_40_40 RDRV_48_48 RDRV_60_60(3)	RDRV_40_40	N/A

Table 1-50: **POD Allowed Attributes *(Cont'd)***

Attributes	IBUF/IBUFE3/IBUFDS/IBUFDSE3			OBUF/OBUFT			IOBUF/IOBUFE3/IOBUFDS/IOBUFDSE3		
	HP I/O		HR I/O	HP I/O		HR I/O	HP I/O		HR I/O
	Allowed Values	Default		Allowed Values	Default		Allowed Values	Default	
IOSTANDARD	POD12_DCI DIFF_POD12_DCI		N/A	POD12_DCI DIFF_POD12_DCI		N/A	POD12_DCI DIFF_POD12_DCI		N/A
SLEW	N/A		N/A	FAST MEDIUM SLOW	SLOW	N/A	FAST MEDIUM SLOW	SLOW	N/A
PRE_EMPHASIS	N/A		N/A	RDRV_240 RDRV_NONE(4)	RDRV_NONE	N/A	RDRV_240 RDRV_NONE(3)	RDRV_NONE	N/A
EQUALIZATION	EQ_LEVEL0, EQ_LEVEL1, EQ_LEVEL2, EQ_LEVEL3, EQ_LEVEL4, EQ_NONE	EQ_NONE	N/A	N/A		N/A	EQ_LEVEL0, EQ_LEVEL1, EQ_LEVEL2, EQ_LEVEL3, EQ_LEVEL4, EQ_NONE	EQ_NONE	N/A
OFFSET_CNTRL	CNTRL_NONE FABRIC	CNTRL_NONE	N/A	N/A		N/A	CNTRL_NONE FABRIC	CNTRL_NONE	N/A
DQS_BIAS(5)	TRUE FALSE	FALSE	N/A	N/A		N/A	TRUE FALSE	FALSE	N/A
ODT	RTT_40 RTT_48 RTT_60(2)	RTT_40	N/A	N/A		N/A	RTT_40 RTT_48 RTT_60(2)(3)	RTT_40	N/A
OUTPUT_ IMPEDANCE	N/A		N/A	RDRV_40_40 RDRV_48_48 RDRV_60_60(4)	RDRV_40_40	N/A	RDRV_40_40 RDRV_48_48 RDRV_60_60(3)	RDRV_40_40	N/A

Notes:

1. The allowed bidirectional configuration combinations for driver output impedance (OUTPUT_IMPEDANCE) and ODT are listed in Table 1-36.
2. ODT = RTT_NONE is not a valid setting for DCI I/O standards.
3. The allowed bidirectional configuration combinations for driver output impedance (OUTPUT_IMPEDANCE), ODT, and PRE_EMPHASIS are listed in Table 1-51.
4. The combinations allowed of driver output impedance (OUTPUT_IMPEDANCE) and PRE_EMPHASIS are listed in Table 1-52.
5. Only applicable to DIFF_POD I/O standards.

Table 1-51 and Table 1-52 lists the allowed combinations of attributes for POD I/O standards.

Table 1-51: **Allowed Combinations of OUTPUT_IMPEDANCE, ODT, and PRE_EMPHASIS**

OUTPUT_IMPEDANCE	ODT	PRE_EMPHASIS
RDRV_40_40 (40Ω)	RTT_40	RDRV_NONE
RDRV_40_40 (40Ω)	RTT_60	RDRV_NONE
RDRV_40_40 (40Ω)	RTT_NONE	RDRV_NONE
RDRV_48_48 (48Ω)	RTT_48	RDRV_NONE
RDRV_48_48 (48Ω)	RTT_NONE	RDRV_NONE
RDRV_60_60 (60Ω)	RTT_40	RDRV_NONE
RDRV_60_60 (60Ω)	RTT_60	RDRV_NONE
RDRV_60_60 (60Ω)	RTT_NONE	RDRV_NONE
RDRV_40_40 (40Ω)	RTT_40	RDRV_240
RDRV_40_40 (40Ω)	RTT_60	RDRV_240
RDRV_40_40 (40Ω)	RTT_NONE	RDRV_240

Table 1-52: **Allowed Combinations of OUTPUT_IMPEDANCE and PRE_EMPHASIS**

OUTPUT_IMPEDANCE	PRE_EMPHASIS
RDRV_40_40 (40Ω)	RDRV_NONE
RDRV_48_48 (48Ω)	RDRV_NONE
RDRV_60_60 (60Ω)	RDRV_NONE
RDRV_40_40 (40Ω)	RDRV_240

LVDS and LVDS_25 (Low Voltage Differential Signaling)

Low-voltage differential signaling (LVDS) is a powerful high-speed interface in many system applications. The I/Os are designed to comply with the EIA/TIA electrical specifications for LVDS system and board design. With the use of an LVDS current-mode driver in the IOBs and the optional internal differential termination feature, the need for external source termination in point-to-point applications is eliminated. UltraScale devices provide a flexible solution for creating an LVDS design.

The LVDS I/O standard is only available in the HP I/O banks. It requires a V_{CCO} to be powered at 1.8V for outputs and for inputs when the optional internal differential termination is implemented.

- DIFF_TERM_ADV = TERM_100
- DIFF_TERM = TRUE

The LVDS_25 I/O standard is only available in the HR I/O banks. It requires a V_{CCO} to be powered at 2.5V for outputs and for inputs when the optional internal differential termination is implemented.

- DIFF_TERM_ADV = TERM_100
- DIFF_TERM = TRUE

Table 1-53: **Available I/O Bank Type**

HR	HP
Available for LVDS_25 only	Available for LVDS only

Transmitter Termination

The LVDS transmitter does not require any external termination. Table 1-54 lists the allowed attributes corresponding to the LVDS current-mode drivers. LVDS current-mode drivers are a true current source and produce the proper (EIA/TIA compliant) LVDS signal.

Receiver Termination

Figure 1-79 is an example of differential termination for an LVDS or LVDS_25 receiver on a board with 50Ω transmission lines.

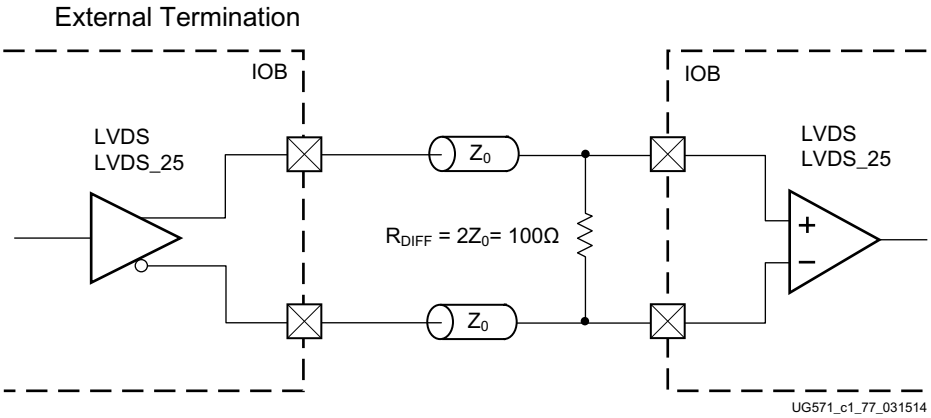

Figure 1-79: **LVDS or LVDS_25 Receiver Termination**

Figure 1-80 is an example of a differential termination for an LVDS or LVDS_25 receiver on a board with 50Ω transmission lines.

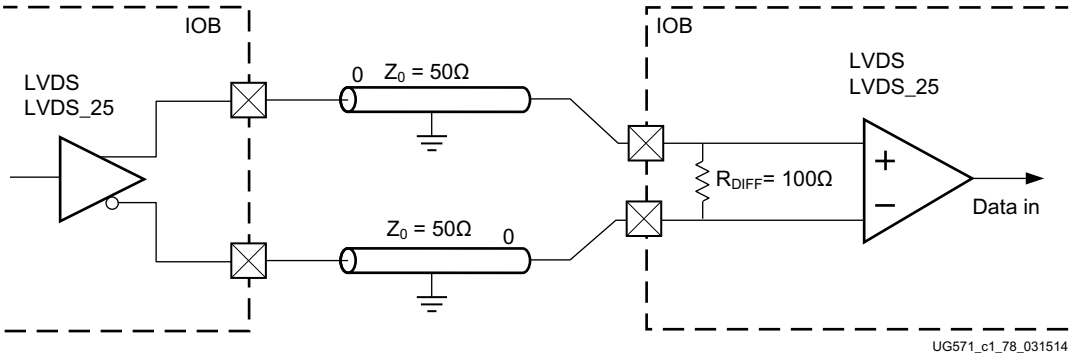

Figure 1-80: **LVDS or LVDS_25 With DIFF_TERM Receiver Termination**

Table 1-54 lists the allowed attributes for the LVDS I/O standards.

Table 1-54: **Allowed Attributes for the LVDS I/O Standards**

Attributes	IBUFDS				OBUFDS			
	HP I/O		HR I/O		HP I/O		HR I/O	
	Allowed Values	Default	Allowed Values	Default	Allowed Values	Default	Allowed Values	Default
IOSTANDARD	LVDS		LVDS_25		LVDS		LVDS_25	
DQS_BIAS	TRUE FALSE(1)(2)	FALSE	N/A		N/A		N/A	
EQUALIZATION	EQ_LEVEL0 EQ_LEVEL1 EQ_LEVEL2 EQ_LEVEL3 EQ_LEVEL4 EQ_NONE(1)	EQ_NONE	EQ_LEVEL0 EQ_LEVEL1 EQ_LEVEL2 EQ_LEVEL3 EQ_LEVEL4 EQ_LEVEL0_DC_BIAS EQ_LEVEL1_DC_BIAS EQ_LEVEL2_DC_BIAS EQ_LEVEL3_DC_BIAS EQ_LEVEL4_DC_BIAS EQ_NONE	EQ_NONE	N/A		N/A	
LVDS_PRE_EMPHASIS	N/A		N/A		TRUE(3) FALSE	FALSE	TRUE(3) FALSE	FALSE
DIFF_TERM	TRUE FALSE	FALSE	TRUE FALSE	FALSE	N/A		N/A	
DIFF_TERM_ADV	TERM_100 TERM_NONE	TERM_NONE	TERM_100 TERM_NONE	TERM_NONE	N/A		N/A	

Notes:

1. The allowed combinations of DQS_BIAS and EQUALIZATION are listed in Table 1-55.
2. DQS_BIAS = TRUE is allowed in AC coupled applications.
3. LVDS_PRE_EMPHASIS = TRUE is only supported in AC coupled applications.

Table 1-55: **Allowed Combinations of DQS_BIAS and EQUALIZATION**

DQS_BIAS	Equalization
FALSE or TRUE (AC coupling)	EQ_LEVEL0, EQ_LEVEL1, EQ_LEVEL2, EQ_LEVEL3, EQ_LEVEL4
FALSE (DC coupling)	EQ_NONE

It is acceptable to have differential inputs such as LVDS and LVDS_25 in I/O banks that are powered at voltage levels other than the nominal voltages required for the outputs of those standards (1.8V for LVDS outputs, and 2.5V for LVDS_25 outputs). However, these criteria must be met:

- The optional internal differential termination is not used.
  - DIFF_TERM_ADV = TERM_NONE
  - DIFF_TERM = FALSE (default).
- The differential signals at the input pins meet the V_{IN} requirements in the *Recommended Operating Conditions* table of the specific UltraScale device data sheet [Ref 1].
- The differential signals at the input pins meet the V_{IDIFF} (min) requirements in the corresponding LVDS or LVDS_25 DC specifications tables of the specific UltraScale device data sheet [Ref 1].

One way to accomplish this criteria is to use an external circuit that both AC-couples and DC-biases the input signals. Figure 1-81 shows an example circuit for providing an AC-coupled and DC-biased circuit for a differential clock input. R_{DIFF} provides the 100Ω differential receiver termination because the internal DIFF_TERM_ADV = TERM_NONE or DIFF_TERM = FALSE. To maximize the input noise margin, all R_{BIAS} resistors should be the same value, essentially creating a V_{ICM} level of $V_{CCO}/2$. Resistors in the 10k–100KΩ range are recommended. The typical values for the AC coupling capacitors C_{AC} are in the range of 100 nF. All components should be placed physically close to the device inputs.

In UltraScale device HP I/O banks, there is an option to use internal bias voltage (DQS_BIAS) in AC-coupled LVDS applications. In such a configuration, EQUALIZATION must be set to EQ_LEVEL0 (1, 2, 3, or 4) for the correct operation, even though EQ_LEVEL0 does not provide equalization. When designing with Vivado Design Suite, the simulation behavior of the DQS_BIAS feature is not modeled when DQS_BIAS is used for DC biasing with an AC-coupled LVDS standard. When an input is 3-stated and the DQS_BIAS is set to TRUE for an LVDS input, the input to the general interconnect is an X in the hardware. Simulation models this condition as an input of 0 to the general interconnect.

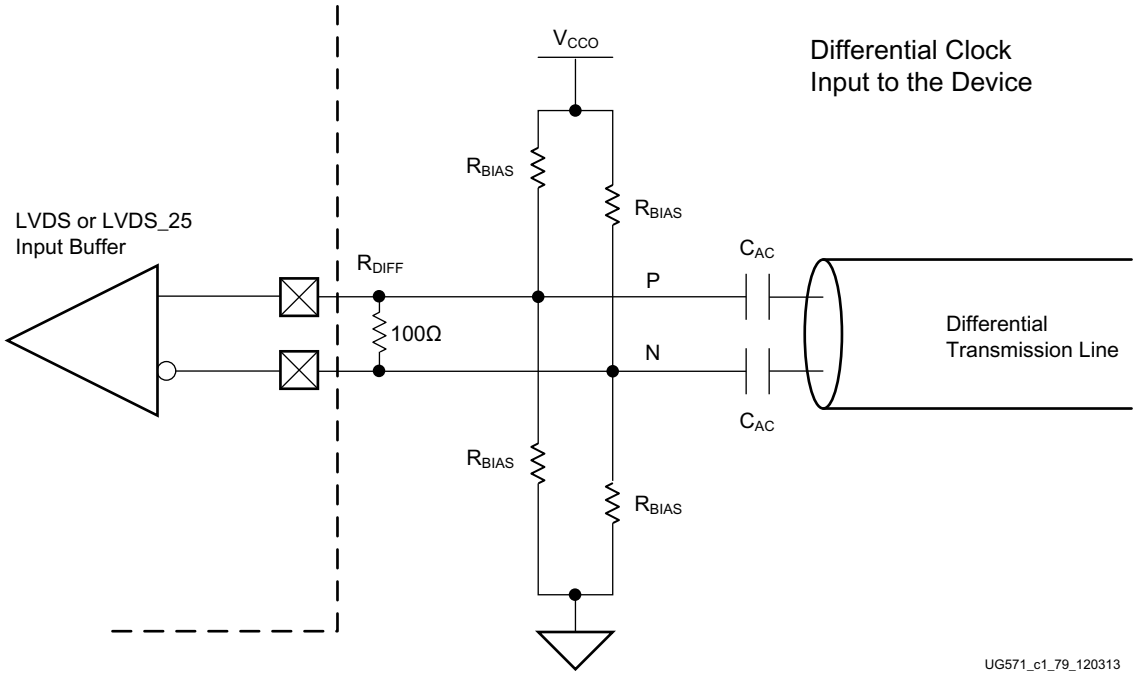

Figure 1-81: **Example Circuit for AC-Coupled and External DC-Biased Differential Clock Input**

RSDS (Reduced Swing Differential Signaling)

Table 1-56: **Available I/O Bank Type**

HR	HP
Available	N/A

Reduced-swing differential signaling (RSDS) is similar to an LVDS high-speed interface using differential signaling. RSDS has a similar implementation to LVDS_25 and is only intended for point-to-point applications. RSDS is only available in HR I/O banks and requires a V_{CCO} voltage level of 2.5V. The IOSTANDARD is called RSDS_25. Table 1-57 summarizes the allowed attributes for the RSDS I/O standard.

Table 1-57: **Allowed Attributes for the RSDS I/O Standard**

Attributes	Primitives		
	IBUFDS or IBUFDS_DIFF_OUT		OBUFDS or OBUFTDS
	Allowed Values	Default	
IOSTANDARD	RSDS_25		
DIFF_TERM	TRUE FALSE	FALSE	N/A
DIFF_TERM_ADV	TERM_NONE TERM_100	TERM_NONE	N/A

Mini-LVDS (Mini Low Voltage Differential Signaling)

Table 1-58: **Available I/O Bank Type**

HR	HP
Available	N/A

Mini-LVDS is a serial, intra-flat panel differential I/O standard that serves as an interface between the timing control function and an LCD source driver. Mini-LVDS inputs require a parallel-termination resistor, either by using a discrete resistor on the PCB, or by using the DIFF_TERM_ADV or DIFF_TERM attributes to enable internal termination. Mini-LVDS is only available in HR I/O banks and requires a V_{CCO} voltage level of 2.5V. The IOSTANDARD is called MINI_LVDS_25. Table 1-59 summarizes the allowed attributes for the Mini-LVDS I/O standard.

Table 1-59: **Allowed Attributes of the Mini-LVDS I/O Standard**

Attributes	Primitives		
	IBUFDS or IBUFDS_DIFF_OUT		OBUFDS or OBUFTDS
	Allowed Values	Default	
IOSTANDARD	MINI_LVDS_25		
DIFF_TERM	TRUE FALSE	FALSE	N/A
DIFF_TERM_ADV	TERM_NONE TERM_100	TERM_NONE	N/A

PPDS (Point-to-Point Differential Signaling)

Table 1-60: **Available I/O Bank Type**

HR	HP
Available	N/A

PPDS is a differential I/O standard for next-generation LCD interface row and column drivers. PPDS inputs require a parallel-termination resistor, either through the use of a discrete resistor on the PCB, or by using the DIFF_TERM_ADV or DIFF_TERM attributes to enable internal termination. PPDS is only available in HR I/O banks and requires a V_{CCO} voltage level of 2.5V. The IOSTANDARD is called PPDS_25. Table 1-61 summarizes the allowed attributes for the PPDS I/O standard.

Table 1-61: **Allowed Attributes for the PPDS I/O Standard**

Attributes	Primitives		
	IBUFDS or IBUFDS_DIFF_OUT		OBUFDS or OBUFTDS
	Allowed Values	Default	
IOSTANDARD	PPDS_25		
DIFF_TERM	TRUE FALSE	FALSE	N/A
DIFF_TERM_ADV	TERM_NONE TERM_100	TERM_NONE	N/A

TMDS (Transition Minimized Differential Signaling)

Table 1-62: **Available I/O Bank Type**

HR	HP
Available	N/A

TMDS is a differential I/O standard for transmitting high-speed serial data used by the DVI and HDMI™ video interfaces. The TMDS standard requires external 50Ω pull-up resistors to 3.3V on the inputs. TMDS inputs do not require parallel input termination resistors. TMDS is only available in HR I/O banks and requires a V_{CCO} voltage level of 3.3V. The IOSTANDARD is called TMDS_33. Table 1-63 summarizes the allowed attributes for the TMDS I/O standard.

Table 1-63: **Allowed Attributes for the TMDS I/O Standard**

Attributes	Primitives	
	IBUFDS or IBUFDS_DIFF_OUT	OBUFDS or OBUFTDS
IOSTANDARD	TMDS_33	

BLVDS (Bus LVDS)

Table 1-64: **Available I/O Bank Type**

HR	HP
Available	N/A

Because LVDS is intended for point-to-point applications, BLVDS is not an EIA/TIA standard implementation and requires careful adaptation of I/O and PCB layout design rules. The primitive supplied in the Vivado Design Suite library for bidirectional LVDS does not use the LVDS current-mode driver, instead, it uses complementary single-ended differential drivers. Therefore, source termination is required. BLVDS is only available in HR I/O banks and requires a V_{CCO} voltage level of 2.5V. The IOSTANDARD is called BLVDS_25. Table 1-65 summarizes the allowed attributes for the BLVDS I/O standard.

Table 1-65: **Allowed Attributes for the BLVDS I/O Standard**

Attributes	Primitives	
	IBUFDS or IBUFDS_DIFF_OUT	OBUFDS, OBUFTDS, IOBUFDS, or IOBUFDS_DIFF_OUT
IOSTANDARD	BLVDS_25	

Figure 1-82 shows the BLVDS transmitter termination.

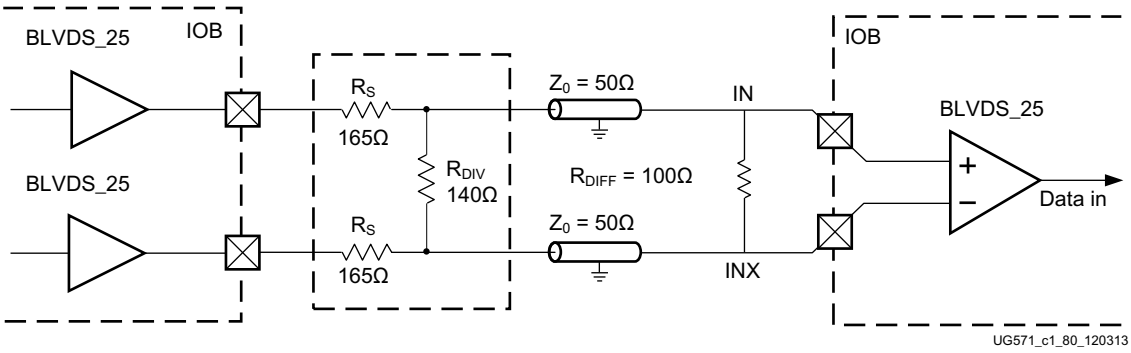

Figure 1-82: **BLVDS Transmitter Termination**

SUB_LVDS

Table 1-66: **Available I/O Bank Type**

HR	HP
Available for SUB_LVDS	Available for SUB_LVDS

Table 1-67 lists the allowed attributes for the SUB_LVDS I/O standards.

Table 1-67: **Allowed Attributes for the SUB_LVDS I/O Standards**

Attributes	Primitives		
	IBUFDS or IBUFDS_DIFF_OUT		OBUFDS or OBUFTDS
	Allowed Values	Default	
IOSTANDARD	SUB_LVDS		
DIFF_TERM	TRUE FALSE	FALSE	N/A
DIFF_TERM_ADV	TERM_NONE TERM_100	TERM_NONE	N/A

SLVS_400

SLVS_400 is supported in HR I/O banks as SLVS_400_25 and in HP I/O banks as SLVS_400_18. SLVS_400 is only supported in receivers.

Table 1-68: **Available I/O Bank Type**

HR	HP
Available for SLVS_400_25 only	Available for SLVS_400_18 only

Table 1-69 lists the allowed attributes for the SLVS_400 I/O standards.

Table 1-69: **Allowed Attributes for the SLVS_400 I/O Standards**

Attributes	Primitives		
	IBUFDS or IBUFDS_DIFF_OUT		OBUFDS or OBUFTDS
	Allowed Values	Default	
IOSTANDARD	SLVS_400_25 for HR I/O banks SLVS_400_18 for HP I/O banks		N/A
DIFF_TERM	TRUE FALSE	FALSE	N/A
DIFF_TERM_ADV	TERM_NONE TERM_100	TERM_NONE	N/A

LVPECL

LVPECL is supported only in HR I/O banks, and is only for receivers.

Table 1-70: **Available I/O Bank Type**

HR	HP
Available	N/A

Table 1-71 lists the allowed attributes for the LVPECL I/O standard.

Table 1-71: **Allowed Attributes for the LVPECL I/O Standard**

Attributes	Primitives	
	IBUFDS or IBUFDS_DIFF_OUT	OBUFDS or OBUFTDS
IOSTANDARD	LVPECL (HR I/O banks only)	N/A

Rules for Combining I/O Standards in the Same Bank

The following rules must be obeyed to combine different input, output, and bidirectional standards in the same bank:

1. **Combining output standards only.** Output standards with the same output V_{CCO} requirement can be combined in the same bank.

   Compatible example:

   SSTL15_I and LVDCI_15 outputs

   Incompatible example:

   SSTL15 (output V_{CCO} = 1.5V) and
   LVCMOS18 (output V_{CCO} = 1.8V) outputs

Only two true differential output I/O standards can be combined in HR I/O banks. LVDS_25 with LVDS_PRE_EMPHASIS = FALSE (default) and LVDS_25 with LVDS_PRE_EMPHASIS = TRUE are considered as two different true-differential output standards in HR I/O banks.

Only one true differential output I/O standard can be used in HP I/O banks. LVDS with LVDS_PRE_EMPHASIS = FALSE (default) and LVDS with LVDS_PRE_EMPHASIS = TRUE are considered as two different true-differential output standards and cannot be combined within the same HP I/O bank.

2. **Combining input standards only.** Input standards with the same V_{CCO} and V_{REF} requirements can be combined in the same bank.

   Compatible example:

   LVCMOS15 and HSTL_II inputs

   Incompatible example:

   LVCMOS15 (input V_{CCO} = 1.5V) and
   LVCMOS18 (input V_{CCO} = 1.8V) inputs

   Incompatible example:

   HSTL_I_DCI_18 (V_{REF} = 0.9V) and
   HSTL_I_DCI (V_{REF} = 0.75V) inputs

3. **Combining input standards and output standards.** Input standards and output standards with the same V_{CCO} requirement can be combined in the same bank.

   Compatible example:

   LVDS_25 output and LVCMOS25 input

   Incompatible example:

   LVDS_25 output (output V_{CCO} = 2.5V) and
   HSTL_I input (input V_{CCO} = 1.5V)

4. **Combining bidirectional standards with input or output standards.** When combining bidirectional I/O with other standards, make sure the bidirectional standard can meet the first three rules.

The implementation tools enforce these design rules.

Table 1-72, summarizes the V_{CCO} and V_{REF} requirements for each supported I/O standard. For more detailed DC specifications, including the recommended operating ranges of the supplies for each supported I/O standard, see the specific UltraScale device data sheet [Ref 1].

Table 1-72: **V_{CCO} and V_{REF} Requirements for Each Supported I/O Standard**

I/O Standard	I/O Bank Availability	V_{CCO} (V)			V_{REF} (V)
		Output	Input	Input with DIFF_TERM_ADV and DIFF_TERM Support	Input
LVTTL	HR	3.3	3.3	N/A	N/A
LVCMOS33	HR	3.3	3.3	N/A	N/A
LVCMOS25	HR	2.5	2.5	N/A	N/A
LVCMOS18	Both	1.8	1.8	N/A	N/A
LVCMOS15	Both	1.5	1.5	N/A	N/A
LVCMOS12	Both	1.2	1.2	N/A	N/A
HSUL_12	Both	1.2	1.2(2)	N/A	0.60
LVDCI_18	HP	1.8	1.8	N/A	N/A
LVDCI_15	HP	1.5	1.5	N/A	N/A
HSUL_12_DCI	HP	1.2	1.2	N/A	0.60
HSLVDCI_18	HP	1.8	Any	N/A	0.90
HSLVDCI_15	HP	1.5	Any	N/A	0.75
HSTL_I	Both	1.5	1.5	N/A	0.75
HSTL_II	HR	1.5	1.5	N/A	0.75
HSTL_I_DCI	HP	1.5	1.5	N/A	0.75
HSTL_I_18	Both	1.8	1.8	N/A	0.90
HSTL_II_18	HR	1.8	1.8	N/A	0.90
HSTL_I_DCI_18	HP	1.8	1.8	N/A	0.90
HSTL_I_12	HP	1.2	1.2	N/A	0.60
HSTL_I_DCI_12	HP	1.2	1.2	N/A	0.60
SSTL18_I	Both	1.8	1.8	N/A	0.90
SSTL18_II	HR	1.8	1.8	N/A	0.90
SSTL15	Both	1.5	1.5	N/A	0.75
SSTL15_R	HR	1.5	1.5	N/A	0.75
SSTL135	Both	1.35	1.35	N/A	0.675
SSTL135_R	HR	1.35	1.35	N/A	0.675
SSTL12	Both	1.2	1.2	N/A	0.60
SSTL18_I_DCI	HP	1.8	1.8	N/A	0.90
SSTL15_DCI	HP	1.5	1.5	N/A	0.75

Table 1-72: **V_{CCO} and V_{REF} Requirements for Each Supported I/O Standard *(Cont'd)***

I/O Standard	I/O Bank Availability	V_{CCO} (V)			V_{REF} (V)
		Output	Input	Input with DIFF_TERM_ADV and DIFF_TERM Support	Input
SSTL135_DCI	HP	1.35	1.35	N/A	0.675
SSTL12_DCI	HP	1.2	1.2	N/A	0.60
DIFF_HSTL_I	Both	1.5	1.5(3)	N/A	N/A
DIFF_HSTL_II	HR	1.5	1.5(3)	N/A	N/A
DIFF_HSTL_I_18	Both	1.8	1.8(3)	N/A	N/A
DIFF_HSTL_II_18	HR	1.8	1.8(3)	N/A	N/A
DIFF_SSTL18_I	Both	1.8	1.8(3)	N/A	N/A
DIFF_SSTL18_II	HR	1.8	1.8(3)	N/A	N/A
DIFF_SSTL15	Both	1.5	1.5(3)	N/A	N/A
DIFF_SSTL15_R	HR	1.5	1.5(3)	N/A	N/A
DIFF_SSTL135	Both	1.35	1.35(3)	N/A	N/A
DIFF_SSTL135_R	HR	1.35	1.35(3)	N/A	N/A
DIFF_SSTL12	Both	1.2	1.2(3)	N/A	N/A
DIFF_HSUL_12	Both	1.2	1.2(4)	N/A	N/A
DIFF_HSTL_I_DCI	HP	1.5	1.5	N/A	N/A
DIFF_HSTL_I_DCI_18	HP	1.8	1.8	N/A	N/A
DIFF_SSTL18_I_DCI	HP	1.8	1.8	N/A	N/A
DIFF_SSTL15_DCI	HP	1.5	1.5	N/A	N/A
DIFF_SSTL135_DCI	HP	1.35	1.35	N/A	N/A
DIFF_SSTL12_DCI	HP	1.2	1.2	N/A	N/A
DIFF_HSUL_12_DCI	HP	1.2	1.2	N/A	N/A
BLVDS_25	HR	2.5	Any	N/A	N/A
LVDS_25	HR	2.5	2.5(1)	2.5	N/A
RSDS_25	HR	2.5	2.5(1)	2.5	N/A
TMDS_33	HR	3.3	Any	N/A	N/A
MINI_LVDS_25	HR	2.5	2.5(1)	2.5	N/A
PPDS_25	HR	2.5	2.5(1)	2.5	N/A
LVDS	HP	1.8	1.8(1)	1.8	N/A
LVPECL	HR	N/A	Any	N/A	N/A
SLVS_400_18	HP	N/A	1.8(1)	1.8	N/A
SLVS_400_25	HR	N/A	2.5(1)	2.5	N/A
SUB_LVDS	Both	1.8	1.8(1)	1.8	N/A
DIFF_HSTL_I_12	HP	1.2	1.2(3)	N/A	N/A

Table 1-72: **V_{CCO} and V_{REF} Requirements for Each Supported I/O Standard *(Cont'd)***

I/O Standard	I/O Bank Availability	V_{CCO} (V)			V_{REF} (V)
		Output	Input	Input with DIFF_TERM_ADV and DIFF_TERM Support	Input
DIFF_POD10	HP	1.0	1.0(3)	N/A	N/A
DIFF_POD12	HP	1.2	1.2(3)	N/A	N/A
DIFF_HSTL_I_DCI_12	HP	1.2	1.2	N/A	N/A
DIFF_POD10_DCI	HP	1.0	1.0	N/A	N/A
DIFF_POD12_DCI	HP	1.2	1.2	N/A	N/A
POD10	HP	1.0	1.0	N/A	0.70
POD12	HP	1.2	1.2	N/A	0.84
POD10_DCI	HP	1.0	1.0	N/A	0.70
POD12_DCI	HP	1.2	1.2	N/A	0.84

Notes:

1. Differential inputs for these standards can be placed in banks with V_{CCO} levels that are different from the required level for outputs. Some important criteria to consider:
   a. The optional internal differential termination is not used, DIFF_TERM_ADV = TERM_NONE or DIFF_TERM = FALSE (default value), unless the V_{CCO} voltage is at the level required for outputs.
   b. The differential signals at the input pins meet the V_{IN} requirements in the *Recommended Operating Conditions* table of the specific UltraScale device data sheet [Ref 1].
   c. The differential signals at the input pins meet the V_{IDIFF} and V_{ICM} requirements in the DC Specifications tables in the specific UltraScale device data sheet [Ref 1]. In some cases, to accomplish this it might be necessary to provide an external circuit to both AC-couple and DC-bias the pins.
2. For these I/O standards, the V_{CCO} input voltage is 1.2V for HP I/O banks or any specified voltage for HR I/O banks.
3. When on-die input termination is used (ODT is set to a value other than RTT_NONE) or when DQS_BIAS = TRUE, the V_{CCO} input voltage is as specified. When ODT = RTT_NONE and DQS_BIAS = FALSE, the V_{CCO} input voltage is any allowed voltage.
4. When on-die input termination is used (ODT value set to something other than RTT_NONE) or when DQS_BIAS is set to TRUE, the V_{CCO} input voltage is 1.2V for HP I/O banks. In HR I/O banks, when DQS_BIAS = FALSE, or in HP I/O banks when ODT = RTT_NONE, the V_{CCO} input voltage is any allowed voltage.

Table 1-73, summarizes the DRIVE and SLEW attribute options, bidirectional buffer availability, and DCI termination type for each supported I/O standard.

Table 1-73: **Attribute Options, Bidirectional Buffer Availability, and DCI Termination Type**

I/O Standard	I/O Bank Type	Output Slew				Output Drive				Bidirectional Buffers[1]	Termination Type[2]	
		HR I/O Banks		HP I/O Banks		HR I/O Banks		HP I/O Banks			Input	Output[3]
		Allowed Values	Default	Allowed Values	Default	Allowed Values	Default	Allowed Values	Default			
LVTTL	HR	SLOW FAST	SLOW	N/A		4, 8, 12, 16	12	N/A		Yes	None	None
LVCMOS33	HR	SLOW FAST	SLOW	N/A		4, 8, 12, 16	12	N/A		Yes	None	None
LVCMOS25	HR	SLOW FAST	SLOW	N/A		4, 8, 12, 16	12	N/A		Yes	None	None
LVCMOS18	Both	SLOW FAST	SLOW	SLOW MEDIUM FAST	SLOW	4, 8, 12, 16	12	2, 4, 6, 8, 12	12	Yes	None	None
LVCMOS15	Both	SLOW FAST	SLOW	SLOW MEDIUM FAST	SLOW	4, 8, 12, 16	12	2, 4, 6, 8, 12	12	Yes	None	None
LVCMOS12	Both	SLOW FAST	SLOW	SLOW MEDIUM FAST	SLOW	4, 8, 12	12	2, 4, 6, 8	12	Yes	None	None
HSUL_12	Both	SLOW FAST	SLOW	SLOW MEDIUM FAST	SLOW	N/A		N/A		Yes	Single[4]	Driver[4]
LVDCI_18	HP	N/A		SLOW MEDIUM FAST	SLOW	N/A		N/A		Yes	None	Driver
LVDCI_15	HP	N/A		SLOW MEDIUM FAST	SLOW	N/A		N/A		Yes	None	Driver
HSUL_12_DCI	HP	N/A		SLOW MEDIUM FAST	SLOW	N/A		N/A		Yes	Single	Driver
HSLVDCI_18	HP	N/A		SLOW MEDIUM FAST	SLOW	N/A		N/A		Yes	None	Driver
HSLVDCI_15	HP	N/A		SLOW MEDIUM FAST	SLOW	N/A		N/A		Yes	None	Driver
HSTL_I	Both	SLOW FAST	SLOW	SLOW MEDIUM FAST	SLOW	N/A		N/A		Yes	Split	Driver
HSTL_II	HR	SLOW FAST	SLOW	N/A		N/A		N/A		Yes	Split	None

Table 1-73: **Attribute Options, Bidirectional Buffer Availability, and DCI Termination Type *(Cont'd)***

I/O Standard	I/O Bank Type	Output Slew				Output Drive				Bidirectional Buffers[1]	Termination Type[2]	
		HR I/O Banks		HP I/O Banks		HR I/O Banks		HP I/O Banks			Input	Output [3]
		Allowed Values	Default	Allowed Values	Default	Allowed Values	Default	Allowed Values	Default			
HSTL_I_DCI	HP	N/A		SLOW MEDIUM FAST	SLOW	N/A		N/A		Yes	Split	Driver
HSTL_I_18	Both	SLOW FAST	SLOW	SLOW MEDIUM FAST	SLOW	N/A		N/A		Yes	Split	Driver
HSTL_II_18	HR	SLOW FAST	SLOW	N/A		N/A		N/A		Yes	Split	None
HSTL_I_DCI_18	HP	N/A		SLOW MEDIUM FAST	SLOW	N/A		N/A		Yes	Split	Driver
HSTL_I_12	HP	N/A		SLOW MEDIUM FAST	SLOW	N/A		N/A		Yes	Split	Driver
HSTL_I_DCI_12	HP	N/A		SLOW MEDIUM FAST	SLOW	N/A		N/A		Yes	Split	Driver
SSTL18_I	Both	SLOW FAST	SLOW	SLOW MEDIUM FAST	SLOW	N/A		N/A		Yes	Split	Driver
SSTL18_II	HR	SLOW FAST	SLOW	N/A		N/A		N/A		Yes	Split	None
SSTL15	Both	SLOW FAST	SLOW	SLOW MEDIUM FAST	SLOW	N/A		N/A		Yes	Split	Driver
SSTL15_R	HR	SLOW FAST	SLOW	N/A		N/A		N/A		Yes	Split	None
SSTL135	Both	SLOW FAST	SLOW	SLOW MEDIUM FAST	SLOW	N/A		N/A		Yes	Split	Driver
SSTL135_R	HR	SLOW FAST	SLOW	N/A		N/A		N/A		Yes	Split	None
SSTL12	Both	SLOW FAST	SLOW	SLOW MEDIUM FAST	SLOW	N/A		N/A		Yes	Split	Driver
SSTL18_I_DCI	HP	N/A		SLOW MEDIUM FAST	SLOW	N/A		N/A		Yes	Split	Driver
SSTL15_DCI	HP	N/A		SLOW MEDIUM FAST	SLOW	N/A		N/A		Yes	Split	Driver

Table 1-73: **Attribute Options, Bidirectional Buffer Availability, and DCI Termination Type *(Cont'd)***

I/O Standard	I/O Bank Type	Output Slew				Output Drive				Bidirectional Buffers[1]	Termination Type[2]	
		HR I/O Banks		HP I/O Banks		HR I/O Banks		HP I/O Banks			Input	Output[3]
		Allowed Values	Default	Allowed Values	Default	Allowed Values	Default	Allowed Values	Default			
SSTL135_DCI	HP	N/A		SLOW MEDIUM FAST	SLOW	N/A		N/A		Yes	Split	Driver
SSTL12_DCI	HP	N/A		SLOW MEDIUM FAST	SLOW	N/A		N/A		Yes	Split	Driver
DIFF_HSTL_I	Both	SLOW FAST	SLOW	SLOW MEDIUM FAST	SLOW	N/A		N/A		Yes	Split	Driver
DIFF_HSTL_II	HR	SLOW FAST	SLOW	N/A		N/A		N/A		Yes	Split	None
DIFF_HSTL_I_18	Both	SLOW FAST	SLOW	SLOW MEDIUM FAST	SLOW	N/A		N/A		Yes	Split	Driver
DIFF_HSTL_II_18	HR	SLOW FAST	SLOW	N/A		N/A		N/A		Yes	Split	None
DIFF_SSTL18_I	Both	SLOW FAST	SLOW	SLOW MEDIUM FAST	SLOW	N/A		N/A		Yes	Split	Driver
DIFF_SSTL18_II	HR	SLOW FAST	SLOW	N/A		N/A		N/A		Yes	Split	None
DIFF_SSTL15	Both	SLOW FAST	SLOW	SLOW MEDIUM FAST	SLOW	N/A		N/A		Yes	Split	Driver
DIFF_SSTL15_R	HR	SLOW FAST	SLOW	N/A		N/A		N/A		Yes	Split	None
DIFF_SSTL135	Both	SLOW FAST	SLOW	SLOW MEDIUM FAST	SLOW	N/A		N/A		Yes	Split	Driver
DIFF_SSTL135_R	HR	SLOW FAST	SLOW	N/A		N/A		N/A		Yes	Split	None
DIFF_SSTL12	Both	SLOW FAST	SLOW	SLOW MEDIUM FAST	SLOW	N/A		N/A		Yes	Split	Driver
DIFF_HSUL_12	Both	SLOW FAST	SLOW	SLOW MEDIUM FAST	SLOW	N/A		N/A		Yes	Single[4]	Driver[4]
DIFF_HSTL_I_DCI	HP	N/A		SLOW MEDIUM FAST	SLOW	N/A		N/A		Yes	Split	Driver

Table 1-73: **Attribute Options, Bidirectional Buffer Availability, and DCI Termination Type *(Cont'd)***

I/O Standard	I/O Bank Type	Output Slew				Output Drive				Bidirectional Buffers[1]	Termination Type[2]	
		HR I/O Banks		HP I/O Banks		HR I/O Banks		HP I/O Banks			Input	Output[3]
		Allowed Values	Default	Allowed Values	Default	Allowed Values	Default	Allowed Values	Default			
DIFF_HSTL_I_DCI_18	HP	N/A		SLOW MEDIUM FAST	SLOW	N/A		N/A		Yes	Split	Driver
DIFF_SSTL18_I_DCI	HP	N/A		SLOW MEDIUM FAST	SLOW	N/A		N/A		Yes	Split	Driver
DIFF_SSTL15_DCI	HP	N/A		SLOW MEDIUM FAST	SLOW	N/A		N/A		Yes	Split	Driver
DIFF_SSTL135_DCI	HP	N/A		SLOW MEDIUM FAST	SLOW	N/A		N/A		Yes	Split	Driver
DIFF_SSTL12_DCI	HP	N/A		SLOW MEDIUM FAST	SLOW	N/A		N/A		Yes	Split	Driver
DIFF_HSUL_12_DCI	HP	N/A		SLOW MEDIUM FAST	SLOW	N/A		N/A		Yes	Single	Driver
BLVDS_25	HR	N/A		N/A		N/A		N/A		Yes	None	None
LVDS_25	HR	N/A		N/A		N/A		N/A		Yes[5]	None	None
RSDS_25	HR	N/A		N/A		N/A		N/A		Yes[5]	None	None
TMDS_33	HR	N/A		N/A		N/A		N/A		Yes[5]	None	None
MINI_LVDS_25	HR	N/A		N/A		N/A		N/A		Yes[5]	None	None
PPDS_25	HR	N/A		N/A		N/A		N/A		Yes[5]	None	None
LVDS	HP	N/A		N/A		N/A		N/A		Yes[5]	None	None
LVPECL	HR	N/A		N/A		N/A		N/A		No	None	None
SLVS_400_18	HP	N/A		N/A		N/A		N/A		No	None	None
SLVS_400_25	HR	N/A		N/A		N/A		N/A		No	None	None
SUB_LVDS	Both	N/A		N/A		N/A		N/A		Yes[5]	None	None
DIFF_HSTL_I_12	HP	N/A		SLOW MEDIUM FAST	SLOW	N/A		N/A		Yes	Split	Driver
DIFF_POD10	HP	N/A		SLOW MEDIUM FAST	SLOW	N/A		N/A		Yes	Single	Driver
DIFF_POD12	HP	N/A		SLOW MEDIUM FAST	SLOW	N/A		N/A		Yes	Single	Driver

Table 1-73: **Attribute Options, Bidirectional Buffer Availability, and DCI Termination Type *(Cont'd)***

I/O Standard	I/O Bank Type	Output Slew				Output Drive				Bidirectional Buffers[1]	Termination Type[2]	
		HR I/O Banks		HP I/O Banks		HR I/O Banks		HP I/O Banks			Input	Output [3]
		Allowed Values	Default	Allowed Values	Default	Allowed Values	Default	Allowed Values	Default			
DIFF_HSTL_I_DCI_12	HP	N/A		SLOW MEDIUM FAST	SLOW	N/A		N/A		Yes	Split	Driver
DIFF_POD10_DCI	HP	N/A		SLOW MEDIUM FAST	SLOW	N/A		N/A		Yes	Single	Driver
DIFF_POD12_DCI	HP	N/A		SLOW MEDIUM FAST	SLOW	N/A		N/A		Yes	Single	Driver
POD10	HP	N/A		SLOW MEDIUM FAST	SLOW	N/A		N/A		Yes	Single	Driver
POD12	HP	N/A		SLOW MEDIUM FAST	SLOW	N/A		N/A		Yes	Single	Driver
POD10_DCI	HP	N/A		SLOW MEDIUM FAST	SLOW	N/A		N/A		Yes	Single	Driver
POD12_DCI	HP	N/A		SLOW MEDIUM FAST	SLOW	N/A		N/A		Yes	Single	Driver

Notes:

1. The bidirectional buffers column describes the I/O standards use of a bidirectional signal.
2. The DCI termination type column describes the type of termination available for the DCI I/O standards. Split refers to the split-termination resistors. Single refers to single resistor termination to V_{CCO}.
3. A value of DRIVER in this column only applies to HP I/O banks
4. INTERM = Single and OUTTERM = DRIVER for HP I/O banks, INTERM = NONE and OUTTERM = NONE for HR I/O banks.
5. The bidirectional configuration on these I/O standards is a fixed impedance structure optimized to 100Ω differential. They are intended to only be used in point-to-point transmissions that do not have turn around timing requirements. Use BLVDS_25 for bus structures.

Simultaneous Switching Outputs

Due to package inductance, each part/package supports a limited number of simultaneous switching outputs (SSOs), particularly when using fast, high-drive outputs. Fast, high-drive outputs should only be used when required by the application.

The SSN predictor tool provides a way of analyzing the amount of noise margin on each I/O pin in a design based on information for the pin (the victim), as well as all other pins (aggressors) in the design. The tool takes into account I/O pin locations, I/O standards, slew rates, and terminations used, and provides a value for the noise margin for each pin based on these characteristics. The noise margin does not include any system-level characteristics such as board trace cross-talk or reflections due to board impedance discontinuities.

Ground or power bounce occurs when a large number of outputs simultaneously switch in the same direction. The output drive transistors all conduct current to a common rail. Low-to-High transitions connect to the V_{CCO} rail, while High-to-Low transitions connect to the GND rail. The resulting cumulative current transient induces a voltage difference across the inductance that exists between the internal and external ground levels, or internal and external V_{CCO} levels. The inductance is associated with bonding wires, package lead frame, die routing, package routing, and ball inductance. Any SSO-induced voltage consequently affects internal switching noise margins and ultimately signal quality.

The SSN predictor results assume that the device is soldered on the PCB and that the board uses sound design practices. The noise margin values do not apply for devices mounted in sockets due to the additional BGA ball inductance introduced by the socket.

Pin Planning to Mitigate SSO Sensitivity

IMPORTANT: *When performing pin planning of a design, it is important to choose I/O pin placements that separate strong outputs and/or SSOs from sensitive inputs and outputs (particularly asynchronous inputs).*

Strong outputs tend to be the class-II versions of HSTL and SSTL drivers, PCI™ variants, and any LVCMOS or LVTTL with drive strengths over 8 mA. Sensitive inputs and outputs can have a low noise margin and tend to be high-speed signals or signals where the swing is reduced by parallel receiver termination. Because localized SSO noise is based on the proximity of signals to one another, it is important to try to separate signals based on the position of the package solder balls. To further reduce potential noise induced from SSOs, outputs should be distributed evenly rather than clustered in one area. SSOs within a bank should be spread across the bank as much as possible. Whenever possible, SSOs should be distributed into multiple banks.

The floorplanning capability in the Vivado Design Suite can help accomplish pin planning to avoid SSO sensitivity issues. By clicking on a package pin in the Package window, a corresponding IOB is highlighted in the Device window. These IOB site types represent the

die pads and show the relative physical location around the die edge. Through the use of the floorplanning tool, intelligent pin placement can be used to separate the die pads of pins. This is implemented by separating the die pads of pins with strong outputs and SSOs from the die pads of pins with sensitive inputs and outputs. SSO effects can also be minimized by adding virtual GND pins and virtual V_{CCO} pins. A virtual GND is created by defining an output pin driven by a logic 0 at the highest drive strength available and connected to GND on the board. Similarly, a virtual V_{CCO} pin is created by defining an output pin driven by a logic 1 at the highest drive strength and connected to V_{CCO} on the board.

SelectIO Logic Resources

Bank Overview

Each I/O bank contains 52 pins that can be used for input, output, or bidirectional operations using single-ended standards appropriate for the bank, which can be either a high-range (HR) I/O bank, or a high-performance (HP) I/O bank. Up to 48 of these pins can be configured as up to 24 differential signaling pin pairs with signaling appropriate for either an HR I/O or an HP I/O bank. The logic associated with each single-ended pin is known as a bit slice, and the differential pin pairs are referenced as a master bit slice for the _P pin and slave bit slice for the _N pin throughout this user guide.

An overview of each bank is shown in Figure 2-1. The input/output control block bit slices can be programmed using either *component* primitives as in previous generations of Xilinx® devices or configured using native PHY primitives where maximum performance is required. Both mechanisms are discussed in this chapter.

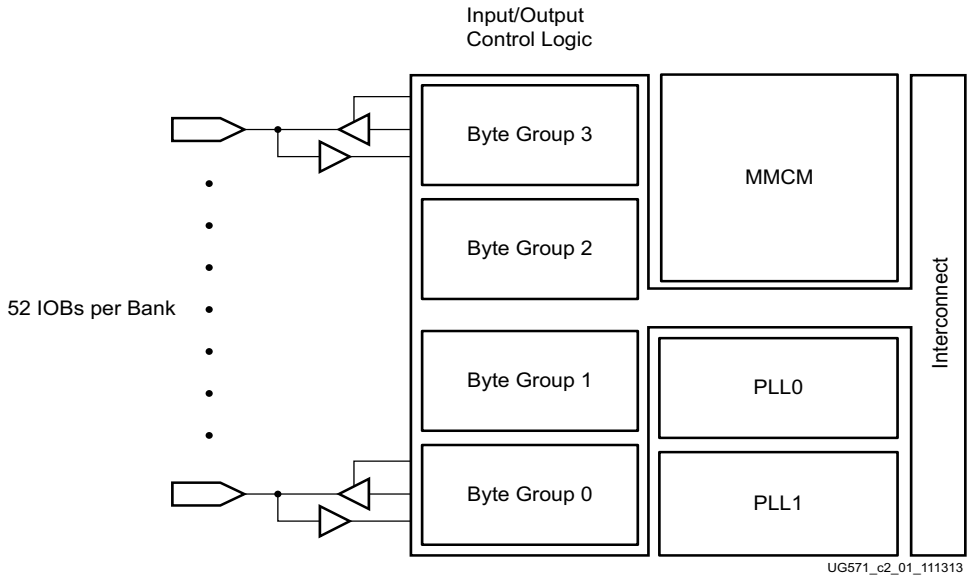

Figure 2-1: **Bank Overview**

Each bank is subdivided into four byte groups, each containing 13 I/O pins as shown in Figure 2-1. Each byte group is further sub-divided into two nibble groups, as shown in

Figure 2-2. The 3-state control bit slice blocks and upper and lower nibble control blocks are only relevant when using the native mode, and are further described in the relevant sections. All bit slices can be used for either single-ended or differential signaling, with the exception of bit slice 12, which is only intended for single-ended signaling. Any single-ended clocks for use with the bit slices should use bit slice 0, and any differential clocks should use bit slices 0 and 1. Other pins can be used for clocks that require access to global clocking resources, as described in the *UltraScale Architecture Clocking Resource User Guide* (UG572) [Ref 9].

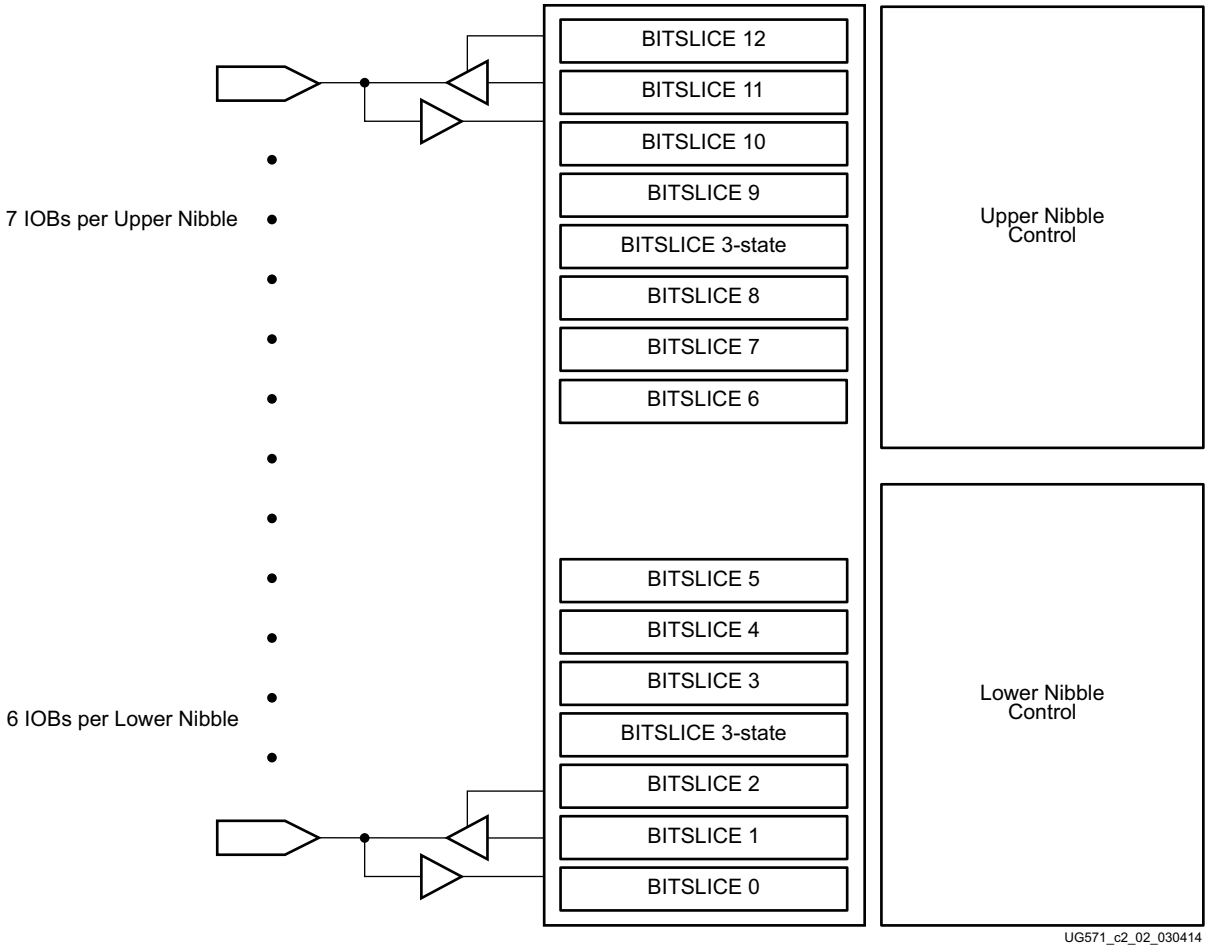

Figure 2-2: **Byte Group Overview**

The two central byte groups (1 and 2) each contain two clock-capable input pins (or pin pairs) that can be used to provide clocking for the byte group or drive one of the clock management mixed-mode clock managers (MMCMs) or phase-locked loops (PLLs). The upper and lower byte groups each contain two clock capable input pins (pin pairs) that can be used for clocking inside the byte group but do not have the capability to drive the MMCMs or PLLs. Clocks can, in addition, be cascaded north and south between byte groups.

Input Using Component Mode

Any input signal can be delayed using the IDELAYE3 primitive and then either forwarded to the device logic directly, or registered in a simple flip-flop or in an input SerDes using a single data rate (SDR) clock or a double data rate (DDR) clock inside the input/output interconnect (IOI).

Input Delay

The IDELAYE3 primitive contains a 512 tap delay line with a maximum value of 1,250 ps. These taps are uncalibrated individually, but the logic to allow a conversion from a fixed value (in ps) to a certain number of taps is built into the I/O control logic. This logic requires a reference clock. No tap-dependent jitter is added by the delay line. The programmed value in FIXED mode is thus maintained over voltage and temperature (VT) when the EN_VTC pin is High. The input delay value can also be manipulated in one of two different ways. In VARIABLE mode, the CE and INC pins are used to manually increment and decrement the delay. At the clock rising edge, if CE and INC are both High, the delay tap value increments by one, or if CE is High and INC is Low, the delay tap value is decremented by one. The EN_VTC pin should be held Low during the delay change command to ensure that any automatic adjustments are stopped. In VAR_LOAD mode, the value present on the CNTVALUEIN bus is loaded into the delay line when CLK rises and LOAD is High. LOAD should only be asserted High for one clock cycle and then held Low for a minimum of eight clock cycles. EN_VTC should again be held Low during this operation to ensure that no contention with the automatic adjustment occurs. The current tap value in the delay line is always available on the CNTVALUEOUT bus.

If delays greater than 1,250 ps are required, an IDELAYE3 can be cascaded with its associated ODELAYE3 in the same bit slice, which in turn can be cascaded with the IDELAYE3 in the bit slice immediately below. This cascade mechanism is shown in Figure 2-3. The function of each IDELAYE3 (or ODELAYE3) is defined by the CASCADE attribute, as shown. The IDELAYE3 (or ODELAYE3) used for cascading are no longer available to the design.

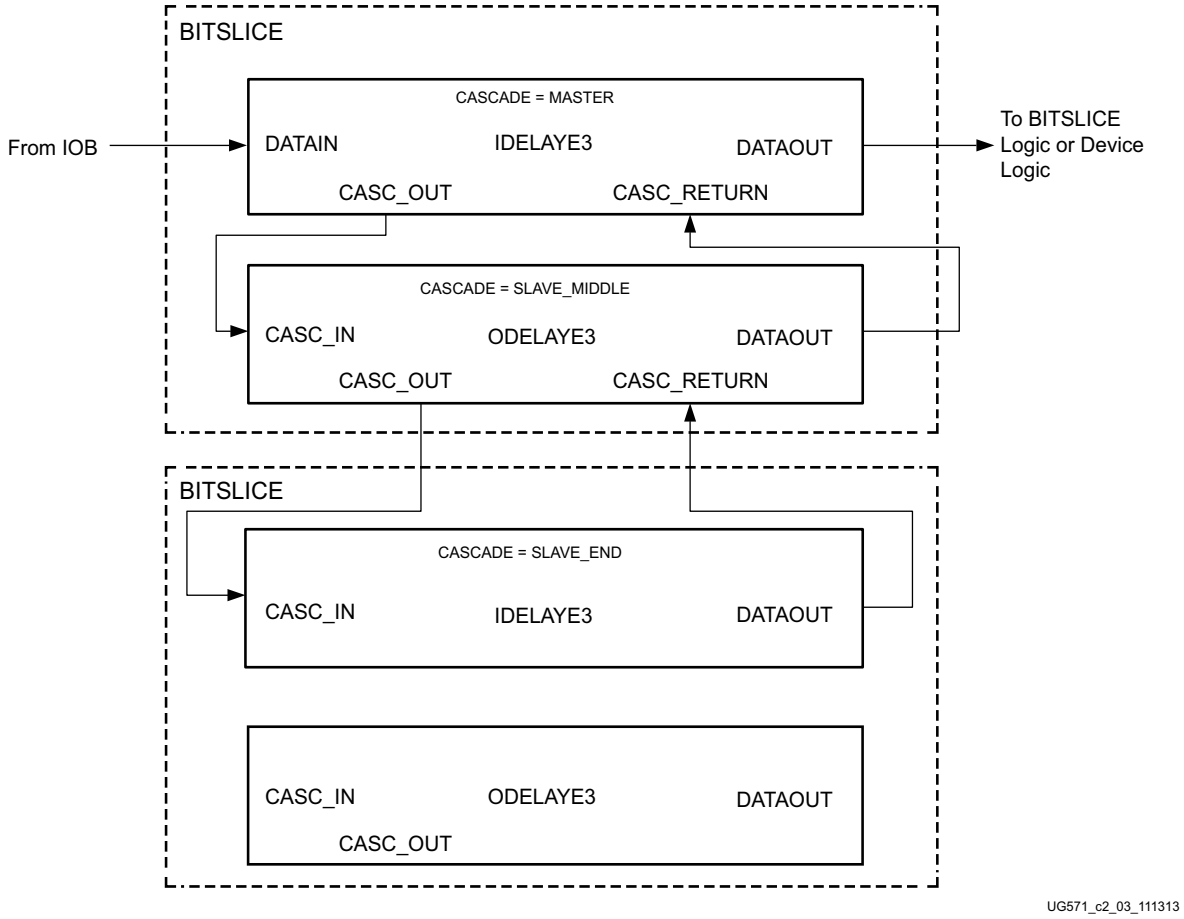

Figure 2-3: **IDELAYE3 Cascading to Two Slave Delays**

Table 2-1 lists the IDELAYE3 ports.

Table 2-1: **IDELAYE3 Ports**

Port	I/O	Description
CASC_RETURN	Input	Cascade delay returning from slave ODELAY DATAOUT.
CASC_IN	Input	Cascade delay from slave ODELAY CASCADE_OUT.
CASC_OUT	Output	Cascade delay to ODELAY in cascade.
CE	Input	Clock enable for the DELAY register clock.
CLK	Input	Clock used to sample LOAD, CE, and INC.
INC	Input	Increment the current delay tap setting when High.
LOAD	Input	Load counter value from CNTVALUEIN when High.
CNTVALUEIN<8:0>	Input	Counter value from logic for tap value to be loaded dynamically.
CNTVALUEOUT<8:0>	Output	Counter value going to logic for monitoring current tap value.
DATAIN	Input	Data input for IDELAY from the programmable logic.
IDATAIN	Input	Data input for IDELAY from the IBUF.

Table 2-1: **IDELAYE3 Ports *(Cont'd)***

Port	I/O	Description
DATAOUT	Output	Delayed data output.
RST	Input	Reset to DELAY_VALUE when High.
EN_VTC	Input	High: Enables IDELAYCTRL to keep delay constant over VT. Low: VT compensation is disabled.

Table 2-2 lists the IDELAYE3 attributes.

Table 2-2: **IDELAYE3 Attributes**

Attribute	Possible Values	Default	Type	Description
DELAY_SRC	DATAIN IDATAIN	IDATAIN	String	Delay line data source.
CASCADE	NONE MASTER SLAVE_MIDDLE SLAVE_END	NONE	String	NONE (default): Delay line is not cascaded. MASTER: Delay line is cascaded with another delay line. SLAVE_MIDDLE: Delay line is cascaded from adjacent delay line and also cascades to another delay line. SLAVE_END: Delay line is the last cascaded delay line.
DELAY_TYPE	FIXED VAR_LOAD VARIABLE	FIXED	String	Delay mode of the DELAY.
DELAY_VALUE	0 to 1250	0	Decimal	TIME mode: Desired value in picoseconds (ps). COUNT mode: Desired value in taps.
REFCLK_FREQUENCY	200.0 to 800.0	300.0	1 significant digit float	Specification of reference clock frequency in MHz.
DELAY_FORMAT	TIME COUNT	TIME	String	When set to TIME, the delay equals the value given in DELAY_VALUE, specified in ps and is calibrated using the REFCLK_FREQUENCY. When set to COUNT, the value given in DELAY_VALUE is not applicable, and the initial tap value will be set 0. This does not give a constant delay as the taps vary with PVT.
UPDATE_MODE	ASYNC SYNC	ASYNC	String	When set to ASYNC, updates to the delay value are independent of the data being received. When set to SYNC, updates require DATAIN (or IDATAIN) transitions to synchronously update the delay with the DATAIN edges. This mode is suitable for clocks or data that is guaranteed to switch on a periodic basis.

If the IDELAYE3 (or ODELAYE3) primitives are instantiated, the IDELAYCTRL module must also be instantiated. There is one IDELAYCTRL module per nibble (eight per bank). The IDELAYCTRL module in conjunction with dedicated bit slice logic continuously calibrates the individual delay lines configured in TIME mode in its region to their programmed value to reduce the effects of process, voltage, and temperature (PVT) variations. The IDELAYCTRL module calibrates IDELAYE3 (and ODELAYE3) using the system-supplied REFCLK. The frequency value of this REFCLK is applied to individual IDELAYE3 (and ODELAYE3) primitives with an attribute. Each delay element in a nibble therefore requires having this attribute set to the same value. Figure 2-4 shows a block diagram of IDELAYCTRL.

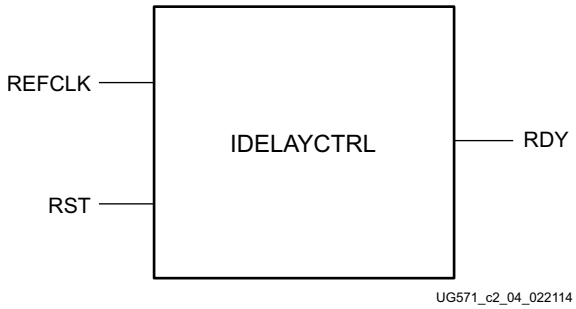

Figure 2-4: **IDELAYCTRL**

Table 2-3 lists the IDELAYCTRL ports.

Table 2-3: **IDELAYCTRL Ports**

Port	I/O	Type	Description
REFCLK	Input	Clock	Reference clock for delay calibration.
RST	Input	Reset	Active-High asynchronous reset for IDELAYCTRL.
RDY	Output	Data	The ready signal goes High to signal that controlled IDELAYE3s and ODELAYE3s are calibrated.

SDR Clocking Without SerDes

SDR input registering inside the bit slice is performed using a flip-flop primitive. This can either be instantiated directly or is inferred by synthesis. Applicable elements are listed.

- FDCE, flip-flip with clock enable and asynchronous clear
- FDPE, flip-flop with clock enable and asynchronous preset
- FDRE, flip-flop with clock enable and synchronous reset
- FDSE, flip-flop with clock enable and synchronous set

DDR Clocking Without SerDes

UltraScale™ devices have dedicated registers in the bit slice to implement input DDR registers. This feature is used by instantiating the IDDRE1 primitive. The IDDRE1 primitive supports these modes of operation:

- OPPOSITE_EDGE
- SAME_EDGE
- SAME_EDGE_PIPELINED

The SAME_EDGE and SAME_EDGE_PIPELINED modes allow designers to transfer falling edge data to the rising edge domain within the bit slice, saving configurable logic block (CLB) and clock resources, and increasing performance. These modes are implemented using the DDR_CLK_EDGE attribute. The following sections describe each of the modes in detail.

OPPOSITE_EDGE Mode

OPPOSITE_EDGE mode, a traditional input DDR solution, is accomplished using a single input in the ILOGIC block. The data is presented to the device logic though the output Q1 on the rising edge of the clock and the output Q2 on the falling edge of the clock. This structure is similar to the 7 series FPGA implementation. Figure 2-5 shows the timing diagram of the input DDR using the OPPOSITE_EDGE mode.

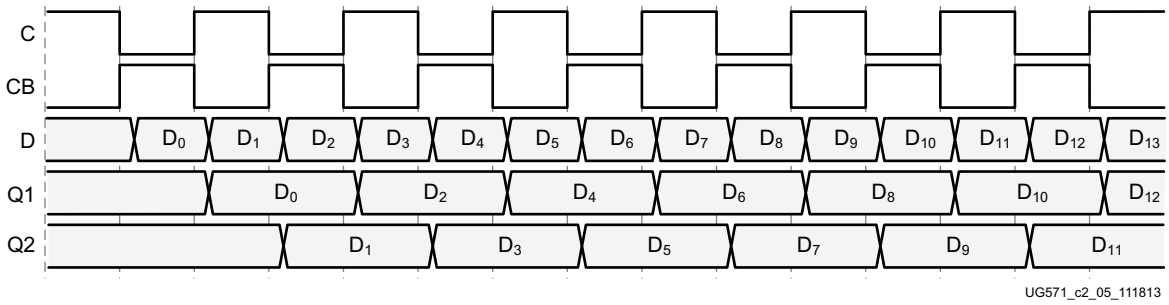

Figure 2-5: **Input DDR Timing in OPPOSITE_EDGE Mode**

SAME_EDGE Mode

In the SAME_EDGE mode, the data is presented into the device logic on the same clock edge. Figure 2-6 shows the timing diagram of the input DDR using the SAME_EDGE mode. In the timing diagram, the output pairs Q1 and Q2 are no longer (0) and (1). Instead, the first pair presented is pair Q1 (0) and Q2 (don't care), followed by pair (1) and (2) on the next clock cycle.

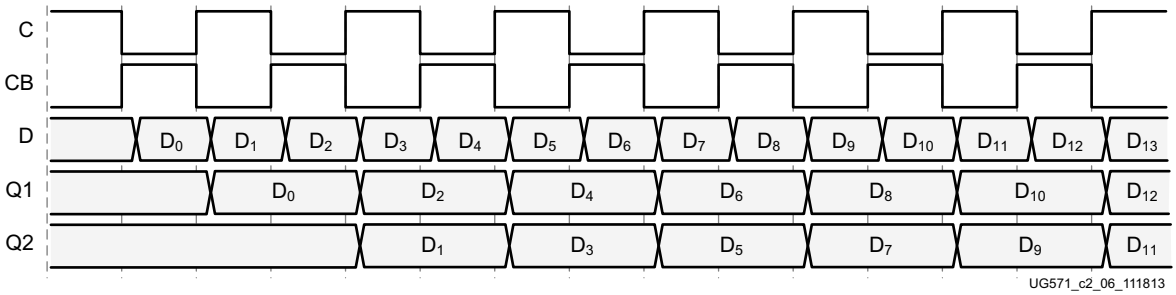

Figure 2-6: **Input DDR Timing in SAME_EDGE Mode**

SAME_EDGE_PIPELINED Mode

In the SAME_EDGE_PIPELINED mode, the data is presented into the device logic on the same clock edge. Unlike the SAME_EDGE mode, the data pair is not separated by one clock cycle. However, additional clock latency is required to remove the separated effect of the SAME_EDGE mode. Figure 2-7 shows the timing diagram of the input DDR using the SAME_EDGE_PIPELINED mode. The output pairs Q1 and Q2 are presented to the device logic at the same time.

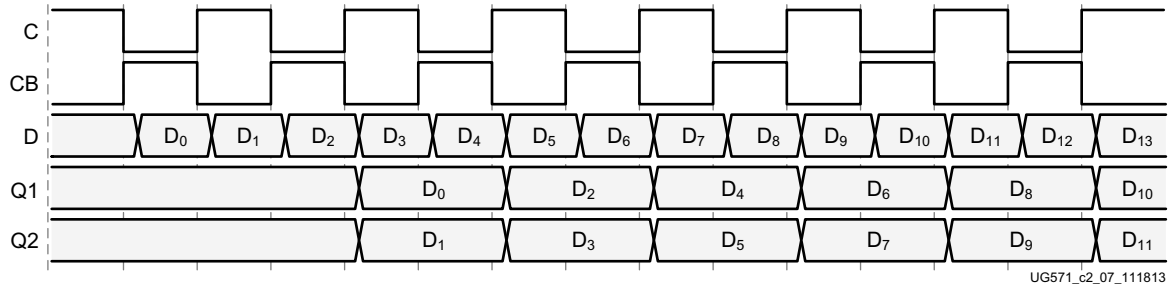

Figure 2-7: **Input DDR Timing in SAME_EDGE_PIPELINED Mode**

Figure 2-8 shows a block diagram of the IDDRE1 primitive.

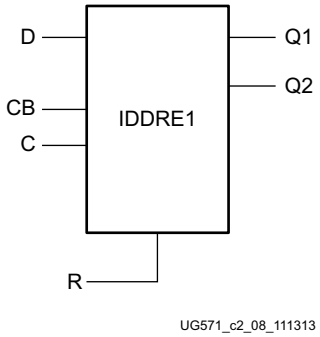

Figure 2-8: **IDDRE1 Primitive Block Diagram**

Table 2-4 lists the IDDRE1 ports.

Table 2-4: **IDDRE1 Ports**

Port	I/O	Description
Q1, Q2	Output	IDDRE1 register outputs.
C	Input	Clock input pin.
CB	Input	Inverted clock input pin.
D	Input	Register input from IOB.
R	Input	Asynchronous reset pin.

Table 2-5 lists the IDDRE1 attributes.

Table 2-5: **IDDRE1 Attributes**

Attribute	Values	Default	Type	Description
DDR_CLK_EDGE	OPPOSITE_EDGE SAME_EDGE SAME_EDGE_PIPELINED	OPPOSITE_EDGE	String	Sets the IDDRE1 mode of operation with respect to clock edge.

Clocking with SerDes

The ISERDESE3 element is available to perform input deserialization. The ISERDESE3 in UltraScale devices is a serial-to-parallel converter with specific clocking and logic features designed to facilitate the implementation of high-speed source-synchronous applications. The ISERDESE3 avoids the additional timing complexities encountered when designing deserializers in the device logic.

The ISERDESE3 can deserialize an incoming signal by 4 in SDR data capture, and by 4 or 8 in DDR data capture. When used for SDR data capture, the valid outputs are every other data output pin. For example, when used as a 1:4 deserializer using an SDR clock, the data width should be set to 8, and the data received is taken from Q0, Q2, Q4, and Q6. Details of which SerDes output pins to use and which value to apply to the DATA_WIDTH attribute are

shown in Table 2-6.

TIP: *The first serial bit received in a word is Q0.*

Table 2-6: **ISERDESE3 Output Connections in SDR and DDR Modes**

SDR or DDR	Required Ratio	DATA_WIDTH Attribute to Apply to ISERDESE3	SerDes Output Data Bits to Use
DDR	1:8	8	Q7, Q6, Q5, Q4, Q3, Q2, Q1, Q0
DDR	1:4	4	Q3, Q2, Q1, Q0
SDR	1:8	N/A	N/A
SDR	1:4	8	Q6, Q4, Q2, Q0
SDR	1:2	4	Q2, Q0

When used, other SerDes ratios are possible with the addition of a simple gearbox that can also emulate a Bitslip feature, if required. The ISERDESE3 also contains a shallow eight entry FIFO that can optionally be used for clock domain transfers. When not used, the FIFO control signals should be connected to GND. When the FIFO is required, the interface is very straightforward. Whenever the FIFO_EMPTY signal is asserted Low, your logic should assert FIFO_RD_ENABLE, then one clock cycle later valid data is available. The timing diagram for operation using the FIFO is shown in Figure 2-9.

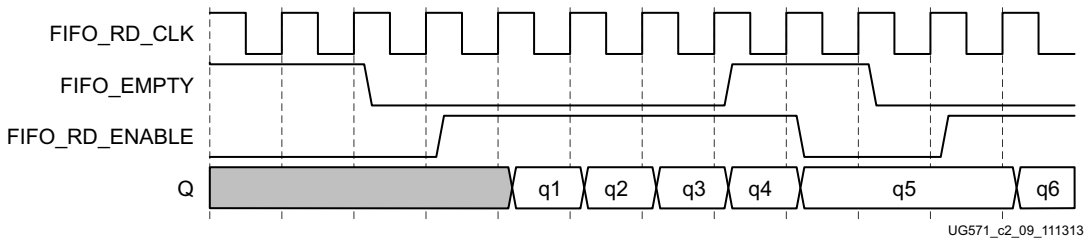

Figure 2-9: **ISERDESE3 Operation using FIFO**

Table 2-7 lists the ISERDESE3 ports.

Table 2-7: **ISERDESE3 Ports**

Port	I/O	Type	Description
CLK	Input	Clock	High-speed clock input. Clock serial input data stream.
CLK_B	Input	Clock	Inversion of CLK.
CLKDIV	Input	Clock	Low-speed divided clock input.
D	Input	Data	Serial input data from IOB or logic.
Q<7:0>	Output	Data	Registered outputs.
RST	Input	Reset	Active-High reset.
FIFO_RD_CLK	Input	Clock	FIFO read clock
FIFO_RD_EN	Input	Enable	Enables reading the FIFO when asserted

Table 2-7: **ISERDESE3 Ports *(Cont'd)***

Port	I/O	Type	Description
FIFO_EMPTY	Output		Indicates the FIFO is approaching empty when asserted
INTERNAL_DIVCLK	Output	Clock	Reserved

Table 2-8 lists the ISERDESE3 attributes.

Table 2-8: **ISERDESE3 Attributes**

Attribute	Values	Default	Type	Description
DATA_WIDTH	4 or 8	8	Decimal	Defines the serial-to-parallel converter width.
FIFO_ENABLE	TRUE FALSE	FALSE	String	The FIFO is used when the attribute is set TRUE and bypassed when the attribute is set FALSE
FIFO_SYNC_MODE	TRUE FALSE	FALSE	String	Set to TRUE when the FIFO write clock and the FIFO read clock are from a common source. Set to FALSE when the FIFO write clock and the FIFO read clock are from separate clock domains.

Output Using Component Mode

Any output signal can be delayed using the ODELAYE3 primitive, having been either forwarded from the device logic directly or registered in a simple flip-flop or an output SerDes using an SDR or DDR clock inside the bit slice.

Output Delay

The ODELAYE3 primitive contains a 512-tap delay line with a maximum value of 1,250 ps. These taps are uncalibrated individually, but the logic to allow a conversion from a fixed value (in ps) to a certain number of taps is built into the I/O control logic. This logic requires a reference clock for calibration and control. No tap-dependent jitter is added by the delay line. The programmed value in FIXED mode is thus maintained over VT when the EN_VTC pin is High. The input delay value can also be manipulated in one of two different ways. In VARIABLE mode, the CE and INC pins are used to manually increment and decrement the delay. At the clock rising edge, if CE and INC are both High, the delay tap value increments by one. If CE is High and INC is Low, the delay tap value decrements by one. LOAD should only be asserted High for one clock cycle and then held Low for a minimum of eight clock cycles. The EN_VTC pin should be held Low during the delay change command to ensure that any automatic adjustments are stopped. In VAR_LOAD mode, the value present on the CNTVALUEIN bus is loaded into the delay line when CLK rises and LOAD is High. EN_VTC should again be held Low during this operation to ensure that no contention with the

automatic adjustment occurs. The current tap value in the delay line is always available on the CNTVALUEOUT bus.

If delays greater than 1,250 ps are required, an ODELAYE3 can be cascaded with the IDELAYE3 in the bit slice immediately below, which in turn can be cascaded with the ODELAYE3 in the same bit slice. This cascade mechanism is shown in Figure 2-10. The function of each ODELAYE3 (or IDELAYE3) is defined by the CASCADE attribute, as shown in Table 2-10.

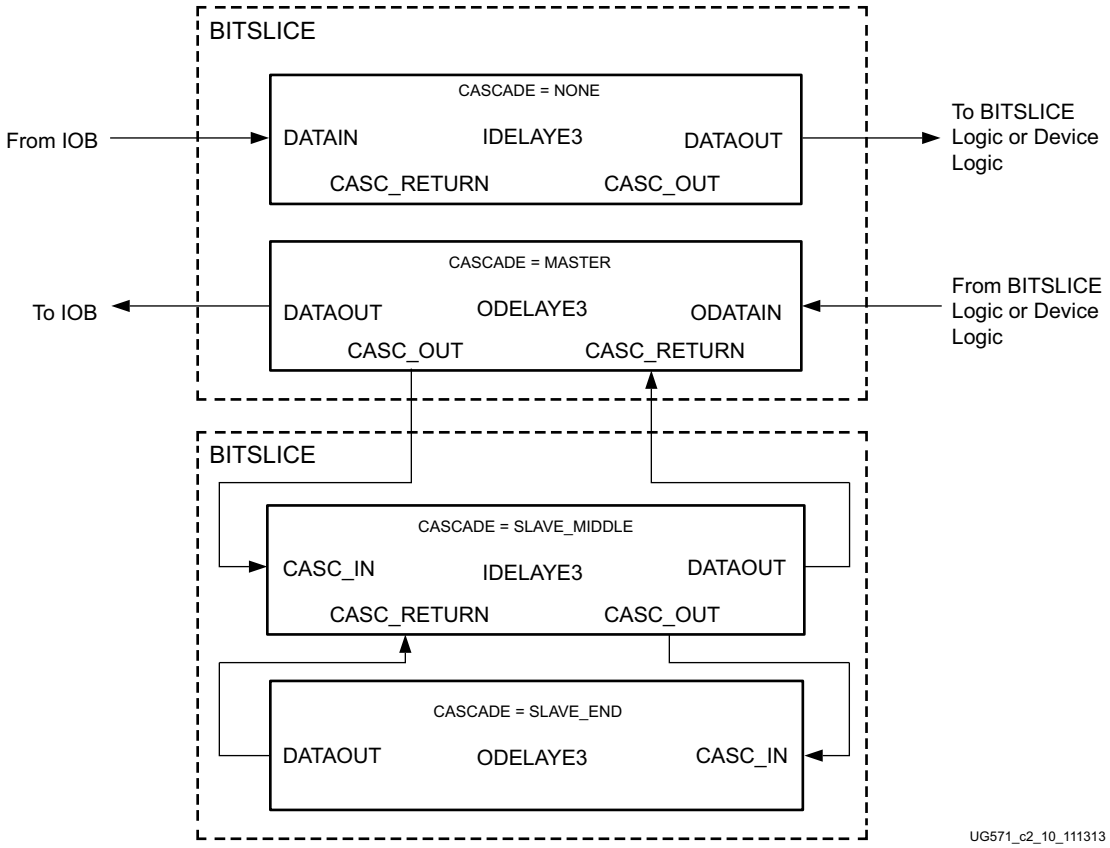

Figure 2-10: **ODELAYE3 Cascading to Two Slave Delays**

Table 2-9 lists the ODELAYE3 ports.

Table 2-9: **ODELAYE3 Ports**

Port	I/O	Description
CASC_RETURN	Input	Cascade delay returning from slave IDELAY DATAOUT.
CASC_IN	Input	Cascade delay from slave IDELAY CASCADE_OUT.
CASC_OUT	Output	Cascade delay to IDELAY in cascade.
CE	Input	Clock enable for the DELAY register clock.
CLK	Input	Delay clock used to sample LOAD and CE INC.
INC	Input	Increments the current delay tap setting.

Table 2-9: **ODELAYE3 Ports *(Cont'd)***

Port	I/O	Description
LOAD	Input	Loads counter value from CNTVALUEIN.
CNTVALUEIN<8:0>	Input	Counter value from device logic for tap value to be loaded dynamically.
CNTVALUEOUT<8:0>	Output	Counter value going to device logic for monitoring tap value.
ODATAIN	Input	Data input for ODELAY from OSERDESE3 or programmable logic.
DATAOUT	Output	Delayed data from data input ports.
RST	Input	Reset to IDELAY_VALUE.
EN_VTC	Input	High: Enables IDELAYCTRL to keep delay over VT. Low: Disables VT compensation.

Table 2-10 lists the ODELAYE3 attributes.

Table 2-10: **ODELAYE3 Attributes**

Attribute	Values	Default	Type	Description
CASCADE	NONE MASTER SLAVE_MIDDLES LAVE_END	NONE	String	None (default): Delay line does not cascade with adjacent delay lines. Master: Delay line is cascaded with other delay lines. Slave_middle: Delay line is cascaded with the adjacent delay line and is also cascaded with other delay lines. Slave_end: Delay line is the last cascaded delay line.
DELAY_TYPE	FIXED VAR_LOAD VARIABLE	FIXED	String	Delay mode of the DELAY.
DELAY_VALUE	0 to 1250	0	Decimal	TIME mode: Desired value in picoseconds (ps). COUNT mode: Desired value in taps.
REFCLK_FREQUENCY	200.0 – 800.0	300.0	1 significant digit float	Specification of reference clock frequency (in MHz).
DELAY_FORMAT	TIME COUNT	TIME	String	When set to TIME, the value given in DELAY_VALUE is specified in ps and is calibrated using the REFCLK_FREQUENCY. When set to COUNT, the value given in DELAY_VALUE is the number of taps to assign to the delay element. This does not give a constant delay as the taps vary with PVT.
UPDATE_MODE	ASYNC SYNC	ASYNC	String	When set to ASYNC, updates are increments or decrements to the delay value independent of the data being received. When set to SYNC, updates require DATAIN (or IDATAIN) transitions to synchronously update the delay with the DATAIN edges. This mode is suitable for clocks or data that is consistently able to switch on a periodic basis.

SDR Clocking Without SerDes

SDR output registering inside the bit slice is performed using a flip-flop primitive. This can either be instantiated directly or is inferred by synthesis. Applicable elements are listed.

- FDCE, flip-flip with clock enable and asynchronous clear
- FDPE, flip-flop with clock enable and asynchronous preset
- FDRE, flip-flop with clock enable and synchronous reset
- FDSE, flip-flop with clock enable and synchronous set

DDR Clocking Without SerDes

UltraScale devices have registers in the bit slice to implement output DDR registers as in previous FPGA generations. This feature is accessed when instantiating the ODDRE1 primitive. DDR multiplexing is automatic when using the ODDRE1. No manual control of the multiplexer select is needed. This control is generated from the clock.

There is only one clock input to the ODDRE1 primitive. Falling-edge data is clocked by a locally inverted version of the input clock.

The ODDRE1 primitive supports only the SAME_EDGE mode of operation. The SAME_EDGE mode allows designers to present both data inputs to the ODDRE1 primitive on the rising edge of the ODDRE1 clock, saving CLB and clock resources, and increasing performance. This mode is also supported for 3-state control. The timing diagram of the output DDR is shown in Figure 2-11.

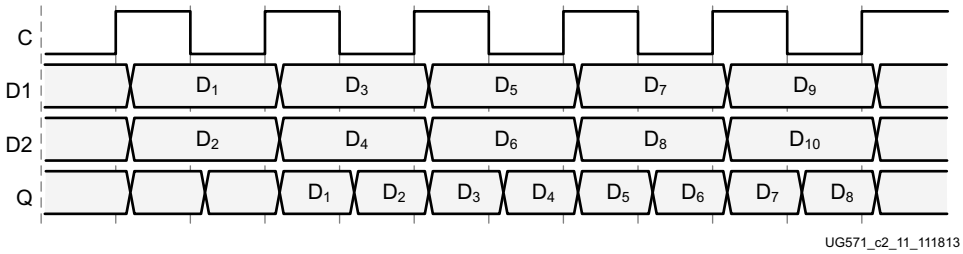

Figure 2-11: **Output DDR Timing**

Figure 2-12 shows a block diagram of the ODDRE1 primitive.

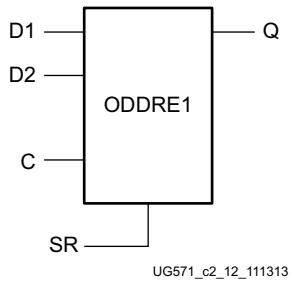

Figure 2-12: **ODDRE1 Primitive Block Diagram**

Table 2-11 lists the ODDRE1 ports.

Table 2-11: **ODDRE1 Ports**

Port	I/O	Description
Q	Output	ODDRE1 register output
C	Input	Clock input pin
D1, D2	Input	ODDRE1 register inputs
SR	Input	Asynchronous set/reset

Table 2-12 lists the ODDRE1 attributes.

Table 2-12: **ODDRE1 Attributes**

Attribute	Values	Default	Type	Description
SRVAL	0 or 1	0	Decimal	Value of Q output configuration after a reset.

Output Clocking with SerDes

The OSERDESE3 element is available to perform output serialization. The OSERDESE3 in UltraScale devices is a parallel-to-serial converter with specific clocking and logic features designed to facilitate the implementation of high-speed source-synchronous applications. The OSERDESE3 avoids the additional timing complexities encountered when designing serializers in the internal device logic.

The OSERDESE3 can serialize an outgoing signal by a 4 in SDR mode, or by a 4 or 8 in DDR mode. When used with SDR clocking, the DATA_WIDTH attribute is to be set to twice the desired width and data to be transmitted should be applied to two pins at a time. For example, the first data to be transmitted should be connected to both D0 and D1; the second bit to be transmitted should be connected to both D2 and D3. Other SerDes ratios are possible with the addition of a gearbox. The full range of possibilities together with the associated attribute settings and required connections are shown in Table 2-13.

TIP: *The data applied to SerDes input D0 is the first bit to be transmitted in all cases.*

Table 2-13: **OSERDESE3 Output Connections in SDR and DDR Modes**

SDR or DDR	Required Ratio	DATA_WIDTH Attribute to Apply to OSERDESE3	Data Bits to Connect to the SerDes
DDR	8:1	8	D7, D6, D5, D4, D3, D2, D1, D0
DDR	4:1	4	0, 0, 0, 0, D3, D2, D1, D0
SDR	8:1	N/A	N/A
SDR	4:1	8	D3, D3, D2, D2, D1, D1, D0, D0
SDR	2:1	4	0, 0, 0, 0, D1, D1, D0, D0

Table 2-14 lists the OSERDESE3 ports.

Table 2-14: **OSERDESE3 Ports**

Port	I/O	Description
CLK	Input	High-speed clock input
CLKDIV	Input	Low-speed divided clock input
D<7:0>	Input	Parallel data inputs for serialization
OQ	Output	Datapath output
RST	Input	Active-High reset
T_OUT	Output	3-state control output to IOB
T	Input	3-state input from IOB

Table 2-15 lists the OSERDESE3 attributes.

Table 2-15: **OSERDESE3 Attributes**

Attribute	Values	Default	Type	Description
DATA_WIDTH	4 or 8	8	Decimal	Defines the parallel-to-serial data converter width.
INIT	`1'b0` `1'b1`	`1'b0`	Binary	Initializes the OSERDESE3 flip-flops to the value specified. For VHDL, use either 0 or 1.

Bidirectional Signaling Using Component Mode

All 52 pins in a bank are capable of bidirectional operation using the same component primitives as described earlier in this chapter.

Input Using Native Mode

The physical layer (PHY) block, BITSLICE, is used for timing control and enables higher data rate reception in UltraScale devices.

For reception, the base building block is the RX_BITSLICE, which is used per pin or pin pair. The six or seven bit slices within a nibble are all controlled by one BITSLICE_CONTROL block, as shown in Figure 2-13 (only six bit slices shown, that is, the lower nibble group in a byte group).

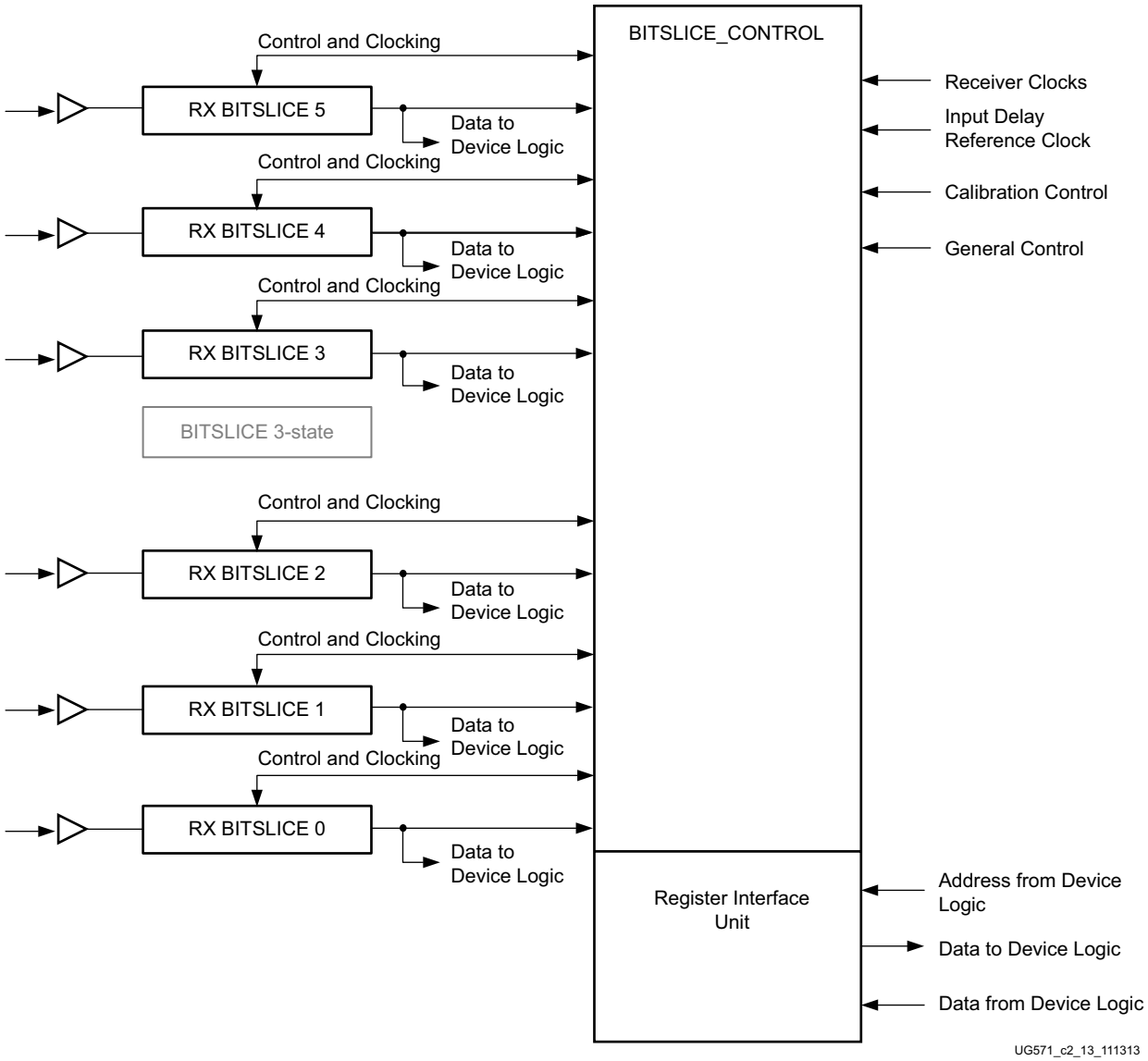

Figure 2-13: **Data Input in Native Mode**

The BITSLICE_CONTROL primitive controls the clocking and characteristics of RX_BITSLICE. Control of BITSLICE_CONTROL is though a register interface unit (RIU), which is a bank of 64 registers each of 16 bits. The RIU register map gives access to all the required delay and control values for the nibble group being programmed. The RIU is shared between the two BITSLICE_CONTROL components that make up a byte group. To differentiate access between two BITSLICE_CONTROL components in the same byte group an RIU_OR component should be used. Receive clocks always use RX_BITSLICE 0 and can be distributed from a bit slice controller to other bit slices within the same bank.

Table 2-16 lists the BITSLICE_CONTROL ports.

Table 2-16: **BITSLICE_CONTROL Ports**

Port	I/O	Description
PLL_CLK	Input	PLL clock input.
REFCLK	Input	Frequency reference clock for delay control.
RST	Input	Asynchronous global reset. Programmable inversion on input.
EN_VTC	Input	Enables voltage and temperature compensation when High.
DLY_RDY	Output	Fixed delay calibration is complete.
VTC_RDY	Output	PHY calibration is complete.
RIU_CLK	Input	Clock input for RIU access.
RIU_ADDR<5:0>	Input	Address input for RIU.
RIU_WR_DATA <15:0>	Input	Data input to RIU.
RIU_RD_DATA <15:0>	Output	Data output from RIU.
RIU_VALID	Output	When High, indicates last data written has been accepted.
RIU_WR_EN	Input	Enables write to RIU when High.
RIU_NIBBLE_SEL	Input	Enables access to the RIU when High
PHY_RDCS0 <3:0>	Input	RANK SELECT. Selects one of four ranks when using a memory interface.
PHY_RDCS1 <3:0>	Input	RANK SELECT. Selects one of four ranks when using a memory interface.
PHY_WRCS0 <3:0>	Input	RANK SELECT. Selects one of four ranks when using a memory interface.
PHY_WRCS1 <3:0>	Input	RANK SELECT. Selects one of four ranks when using a memory interface.
TBYTE_IN<3:0>	Input	Output enable for 3-state control and WClkgen when using a memory interface.
PHY_RDEN<3:0>	Input	Read burst enable when using a memory interface.
DYN_DCI<6:0>	Output	Direct control of IOB DCI when using a memory interface.
CLK_FROM_EXT	Input	Inter-byte clock coming from north or south BITSLICE_CONTROL.
CLK_TO_EXT_NORTH	Output	Inter-byte clock going to north BITSLICE_CONTROL.

Table 2-16: **BITSLICE_CONTROL Ports *(Cont'd)***

Port	I/O	Description
CLK_TO_EXT_SOUTH	Output	Inter-byte clock going to south BITSLICE_CONTROL.
PCLK_NIBBLE_IN	Input	Intra-byte DQS strobes/clock from other control block.
NCLK_NIBBLE_IN	Input	Intra-byte DQS strobes/clock from other control block.
PCLK_NIBBLE_OUT	Output	Intra-byte DQS strobes/clock to other control block.
NCLK_NIBBLE_OUT	Output	Intra-byte DQS strobes/clock to other control block.
RX_BIT_CTRL_OUTx<39:0>	Output	Output bus from BITSLICE_CONTROL to a bit slice in position x in nibble (x = 0 to 6).
RX_BIT_CTRL_INx<39:0>	Input	Input bus to BITSLICE_CONTROL from a bit slice in position x in nibble (x = 0 to 6).
TX_BIT_CTRL_OUTx<39:0>	Output	Output bus to a bit slice in position x in the nibble (x = 0 to 6).
TX_BIT_CTRL_INx<39:0>	Input	Input bus from a bit slice in position x in nibble (x = 0 to 6).
TX_BIT_CTRL_OUT_TRI<39:0>	Output	Output bus to a 3-state bit slice.
TX_BIT_CTRL_IN_TRI<39:0>	Input	Input bus from a 3-state bit slice.

Table 2-17 lists the BITSLICE_CONTROL attributes.

Table 2-17: **BITSLICE_CONTROL Attributes**

Attribute	Values	Default	Type	Description
EN_OTHER_PCLK	TRUE FALSE	FALSE	String	TRUE: Selects the PCLK from the other BITSLICE_CONTROL in the nibble. FALSE: Other BITSLICE_CONTROL PCLK is not used.
EN_OTHER_NCLK	TRUE FALSE	FALSE	String	TRUE: Selects the NCLK from the other BITSLICE_CONTROL in the nibble. FALSE: Other BITSLICE_CONTROL NCLK is not used.
SERIAL_MODE	TRUE FALSE	FALSE	String	TRUE: The input clock for a data receiver comes from an external source through a PLLE3. For example, an SGMII interface. FALSE: The input clock for a data receiver comes from RX_BITSLICE 0.
RX_CLK_PHASE_P	SHIFT_0 SHIFT_90	SHIFT_0	String	SHIFT_90 shifts Read CLK by 90° relative to read DQ during the calibration process.
RX_CLK_PHASE_N	SHIFT_0 SHIFT_90	SHIFT_0	String	SHIFT_90 shifts Read CLK by 90° relative to read DQ during the calibration process.
INV_RXCLK	TRUE FALSE	FALSE	String	Invert clock path from IOB to upper RX_BITSLICE.

Table 2-17: **BITSLICE_CONTROL Attributes *(Cont'd)***

Attribute	Values	Default	Type	Description
TX_GATING	DISABLE ENABLE	DISABLE	String	Clock gating in WClkgen.
RX_GATING	DISABLE ENABLE	DISABLE	String	Read DQS gating.
READ_IDLE_COUNT[5:0]	0 to 63	0	Decimal	Gap count between read bursts for ODT control counter.
DIV_MODE	DIV2 DIV4	DIV2	String	Controller DIV2 (1:4 input SerDes) or DIV4 (1:8 input SerDes) mode.
REFCLK_SRC	PLLCLK REFCLK	PLLCLK	String	Selects the input clock for the delay control.
ROUNDING_FACTOR	1, 2, 4, 8, 16, 32, 64, 128	16	Decimal	$2^{\{1,2,3,4,5,6,7\}}$ for rounding factor.
CTRL_CLK	EXTERNAL	EXTERNAL	String	EXTERNAL: RIU_CLK from external source.
EN_CLK_TO_EXT_NORTH	ENABLE DISABLE	DISABLE	String	Enable clock forwarding to north for inter-byte clocking.
EN_CLK_TO_EXT_SOUTH	ENABLE DISABLE	DISABLE	String	Enable clock forwarding to south for inter-byte clocking.
EN_DYN_ODLY_MODE	TRUE FALSE	FALSE	String	Enables dynamic output delay mode when TRUE.
SELF_CALIBRATE	ENABLE DISABLE	ENABLE	String	Enables or disables the built-in self-calibration feature of the nibble group being controlled by this BITSLICE_CONTROL.
IDLY_VT_TRACK	TRUE FALSE	TRUE	String	Globally enables or disables VT tracking for the input delays associated with this controller.
ODLY_VT_TRACK	TRUE FALSE	TRUE	String	Globally enables or disables VT tracking for the output delays associated with this controller.
QDLY_VT_TRACK	TRUE FALSE	TRUE	String	Globally enables or disables VT tracking for the clock delays associated with this controller.
RXGATE_EXTEND	TRUE FALSE	FALSE	String	Reserved for use by the memory interface generator (MIG) memory controller.

Table 2-18 lists the register interface unit ports (RIU_OR).

Table 2-18: **RIU_OR Ports**

Port	I/O	Description
RIU_RD_DATA_UPP<15:0>	Input	Connect to RIU_RD_DATA of the upper nibble BITSLICE_CONTROL
RIU_RD_DATA_LOW<15:0>	Input	Connect to RIU_RD_DATA of the lower nibble BITSLICE_CONTROL
RIU_RD_VALID_UPP	Input	Connect to RIU_VALID of the upper nibble BITSLICE_CONTROL
RIU_RD_VALID_LOW	Input	Connect to RIU_VALID of the lower nibble BITSLICE_CONTROL
RIU_RD_DATA<15:0>	Output	Combined RIU data bus to interconnect logic
RIU_RD_VALID	Output	Combined RIU read valid signal to interconnect logic

The RX_BITSLICE contains input delays that can be continuously corrected for VT variation by BITSLICE_CONTROL, deserialization logic for either 1:2, 1:4, or 1:8, and a shallow FIFO to allow connection to another clock domain. A block diagram of RX_BITSLICE is shown in Figure 2-14.

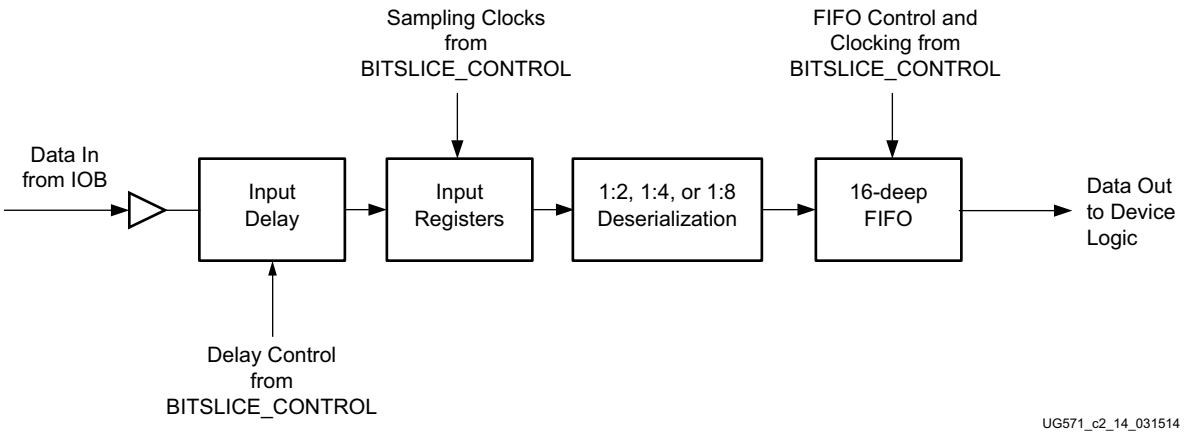

Figure 2-14: **RX_BITSLICE Block Diagram**

Table 2-19 lists the RX_BITSLICE ports.

Table 2-19: **RX_BITSLICE Ports**

Port	I/O	Description
CE	Input	Clock enable for the IDELAY register clock.
CLK	Input	DELAY Clock used to sample LOAD, CE INC.
INC	Input	Increment the current delay tap setting.
LOAD	Input	Load the CNTVALUE from CNTVALUEIN.
CNTVALUEIN<8:0>	Input	Counter value from internal device logic for tap value to be loaded dynamically.

Table 2-19: **RX_BITSLICE Ports *(Cont'd)***

Port	I/O	Description
CNTVALUEOUT<8:0>	Output	Extended counter value going to internal device logic for monitoring tap value.
DATAIN	Input	Input signal from the IBUF.
Q<7:0>	Output	Registered output data from FIFO.
RST_DLY	Input	Reset the internal DELAY to value defined in DELAY_VALUE.
RST	Input	Asynchronous assertion, synchronous deassertion reset signal for ISERDESE3.
EN_VTC	Input	High: Enables IDELAYCTRL to keep delay over VT. Low: VT compensation is disabled.
RX_BIT_CTRL_IN<39:0>	Input	Receiver input control bus from BITSLICE_CONTROL.
RX_BIT_CTRL_OUT<39:0>	Output	Receiver output bus to BITSLICE_CONTROL.
EN_VTC_EXT	Input	(Optional) Extended delay enable for stable delay as voltage and temperature change.
TX_BIT_CTRL_IN<39:0>	Input	Control signals from BITSLICE_CONTROL.
TX_BIT_CTRL_OUT<39:0>	Output	Control signals from BITSLICE_CONTROL.
FIFO_RD_CLK	Input	Clock, read clock for this bit's FIFO.
FIFO_RD_EN	Input	Enable FIFO enable for this bit's FIFO.
FIFO_EMPTY	Output	Data, FIFO empty flag for this bit.
FIFO_WRCLK_OUT	Output	Clock, FIFO source synchronous write clock out to the device logic. Only valid for RX_BITSLICE 0.
CE_EXT	Input	(Optional) Extended (cascaded delay) clock enable for the DELAY register clock.
CLK_EXT	Input	(Optional) Extended (cascaded delay) DELAY clock used to sample LOAD CE and INC.
INC_EXT	Input	(Optional) Extended (cascaded delay) increments the current delay tap setting.
RST_DLY_EXT	Input	(Optional) Reset the internal extended DELAY to the value defined in DELAY_VALUE.
LOAD_EXT	Input	(Optional) Extended (cascaded delay) loads the CNTVALUE from CNTVALUEIN.
CNTVALUEIN_EXT<8:0>	Input	(Optional) Extended (cascaded delay) counter value from device logic for tap value that to be loaded dynamically.
CNTVALUEOUT_EXT<8:0>	Output	(Optional) Extended (cascaded delay) counter value going to device logic for monitoring tap value.

Table 2-20 lists the RX_BITSLICE attributes.

Table 2-20: **RX_BITSLICE Attributes**

Attribute	Values	Default	Type	Description
CASCADE	TRUE FALSE	FALSE	String	TRUE: Enables cascading of IDELAY and ODELAY lines to get a total of 2.5 ns delay. The extended delay is controlled by the _EXT pins. FALSE: Only use IDELAY delay line with a maximum of 1.25 ns.
DATA_WIDTH	4 8	8	Decimal	Defines the width of the serial-to-parallel converter.
DATA_TYPE	NONE DATA CLOCK DATA_AND_CLOCK	NONE	String	Defines whether the input pin is carrying a clock or data, or a clock that is also used as data.
DELAY_TYPE	FIXED VAR_LOAD VARIABLE	FIXED	String	Delay mode of the DELAY.
DELAY_VALUE	0 – 1250	0	Decimal	TIME mode: Desired value in picoseconds (ps). COUNT mode: Desired value in taps.
DELAY_VALUE_EXT	0 – 1250	0	Decimal	TIME mode: Desired value in picoseconds (ps). COUNT mode: Desired value in taps.
REFCLK_FREQUENCY	300.0 – 2400.0	300.0	1 significant digit float	Specification of reference clock frequency in MHz.
DELAY_FORMAT	TIME COUNT	TIME	String	When set to TIME, the value given in DELAY_VALUE is specified in ps and is calibrated using the REFCLK_FREQUENCY. When set to COUNT, the value given in DELAY_VALUE is the number of taps to assign to the delay element.
UPDATE_MODE	ASYNC SYNC	ASYNC	String	When set to ASYNC, updates are increments and decrements to the delay value. When set to SYNC, updates require DATAIN (or IDATAIN) switching to synchronously update the delay with the DATAIN edges.
UPDATE_MODE_EXT	ASYNC SYNC	ASYNC	String	When set to ASYNC, updates are increments and decrements to the delay value. When set to SYNC, updates require DATAIN (or IDATAIN) switching to synchronously update the delay with the DATAIN edges.
FIFO_SYNC_MODE	TRUE FALSE	FALSE	BOOLSTRING	Set this to TRUE when the internal write clock and the FIFO_RD_CLK are coming from a common source, all clock timing from write to read must be met. Set this to FALSE when the FIFO write clock and the FIFO read clock are not on a common clock domain.

Output Using Native Mode

For data transmission, the base building block is TX_BITSLICE, which is used per pin or pin pair. The six or seven bit slices within a nibble are all controlled by one BITSLICE_CONTROL block, as shown in Figure 2-15.

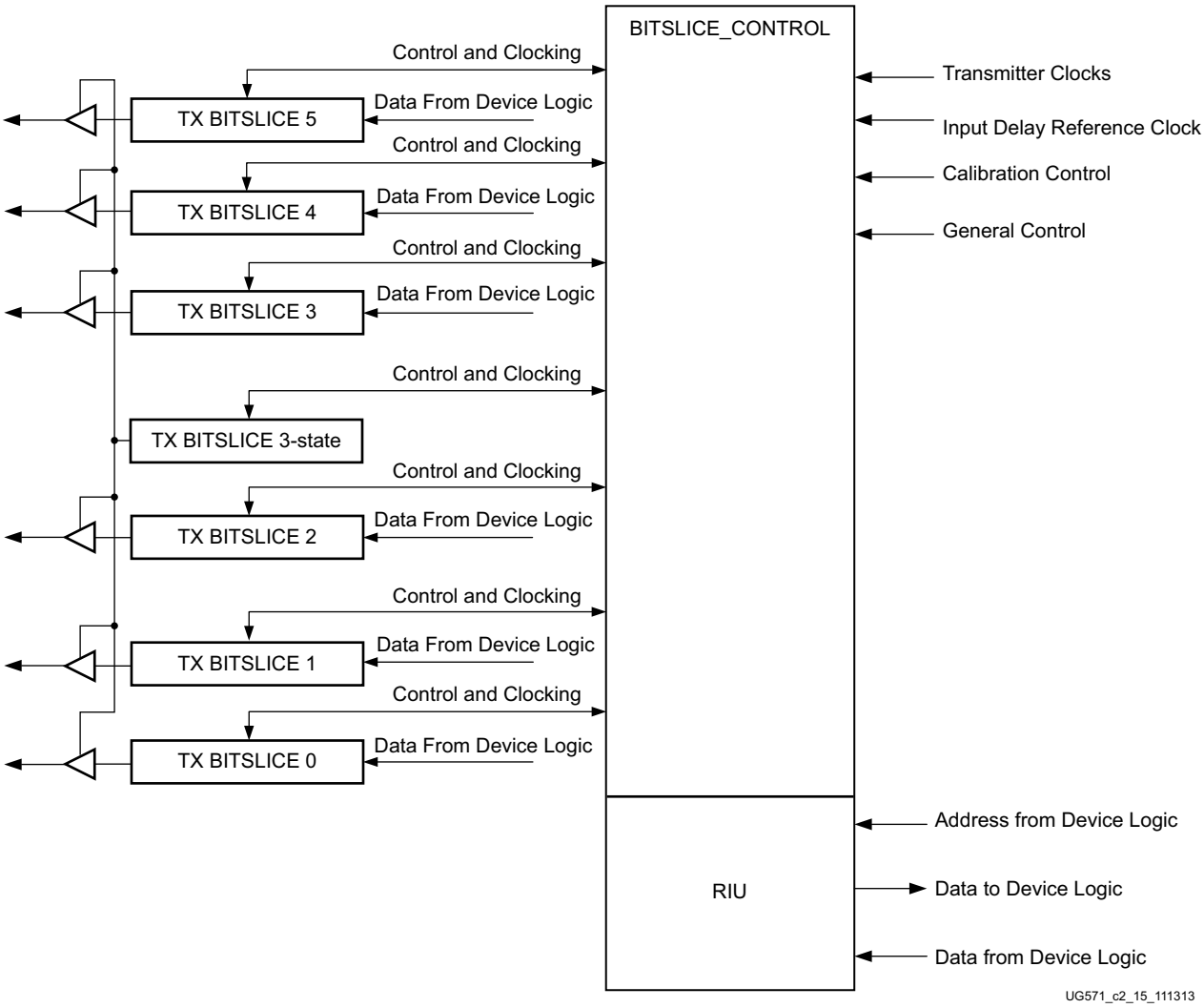

Figure 2-15: **Native Mode Data Transmission**

TX_BITSLICE contains output delays that can be continuously corrected for VT variation by BITSLICE_CONTROL and serialization logic for either 2:1, 4:1, or 8:1. A block diagram of TX_BITSLICE is shown in Figure 2-16.

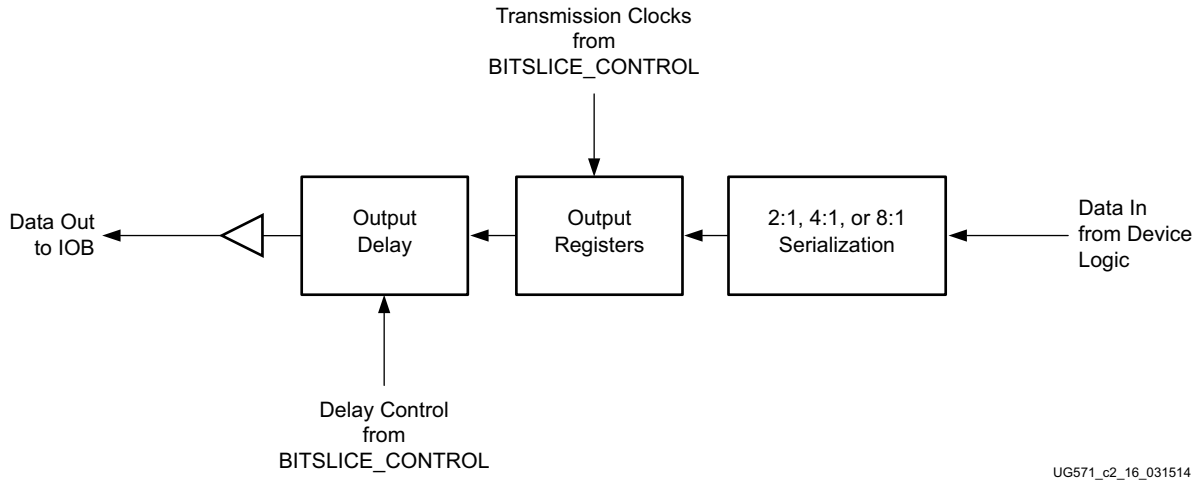

Figure 2-16: **TX_BITSLICE Block Diagram**

Table 2-21 lists the TX_BITSLICE ports.

Table 2-21: **TX_BITSLICE Ports**

Port	I/O	Description
CE	Input	Clock enable for the DELAY register clock.
CLK	Input	DELAY clock used to sample LOAD and CE INC.
INC	Input	Increments the current delay tap setting.
LOAD	Input	Loads CNTVALUE from CNTVALUEIN.
CNTVALUEIN<8:0>	Input	Counter value from device logic for tap value to be loaded dynamically.
CNTVALUEOUT<8:0>	Output	Counter value going to device logic for monitoring tap value.
O	Output	Serialized output going to output buffer.
D<7:0>	Input	Data from device logic.
RST_DLY	Input	Resets the internal ODELAY to the value defined in DELAY_VALUE.
RST	Input	Asynchronous reset, synchronous release for OSERDESE3.
T	Input	Legacy T byte input from device logic.
T_OUT	Output	Byte group 3-state output.
TBYTE_IN	Input	Byte group 3-state input.
EN_VTC	Input	High: Enables IDELAYCTRL to keep delay over VT. Low: Disables VT compensation.
TX_BIT_CTRL_IN<39:0>	Input	Input bus from BITSLICE_CONTROL.
TX_BIT_CTRL_OUT<39:0>	Output	Output bus to BITSLICE_CONTROL.
RX_BIT_CTRL_IN<39:0>	Input	Input bus from BITSLICE_CONTROL.
RX_BIT_CTRL_OUT<39:0>	Output	Output bus to BITSLICE_CONTROL.

Table 2-22 lists the TX_BITSLICE attributes.

Table 2-22: **TX_BITSLICE Attributes**

Attributes	Values	Default	Type	Description
DATA_WIDTH	4 or 8	8	Decimal	Defines the parallel data input width.
TBYTE_CTL	TBYTE_IN or T	TBYTE_IN	String	Selects between the T and TBYTE_IN inputs. In OSERDESE3 mode only, TYBYTE_CTL defaults to TBYTE_IN.
INIT	`1'b0` or `1'b1`	`1'b1`	Binary	Defines initial O value.
DELAY_TYPE	FIXED VAR_LOAD VARIABLE	FIXED	String	Delay mode of the DELAY.
DELAY_VALUE	0 – 1250	0	Decimal	TIME mode: Desired value in picoseconds (ps). COUNT mode: Desired value in taps.
REFCLK_FREQUENCY	300.0 – 2400.0	300.0	1 significant digit float	Specification of reference clock frequency (in MHz).
OUTPUT_PHASE_90	TRUE or FALSE	FALSE	String	Delays output phase by 90°.
DELAY_FORMAT	TIME COUNT	TIME	String	When set to TIME, the value given in DELAY_VALUE is specified in ps and is calibrated using the REFCLK_FREQUENCY. When set to COUNT, the value given in DELAY_VALUE is the number of taps to assign to the delay element.
UPDATE_MODE	ASYNC SYNC	ASYNC	String	When set to ASYNC, updates are increments and decrements to the delay value. When set to SYNC, updates require DATAIN (or IDATAIN) switching to synchronously update the delay with the DATAIN edges.
ENABLE_PRE_EMPHASIS	TRUE FALSE	FALSE	String	Used in conjunction with attributes on the IOB to enable and disable pre-emphasis.

Bidirectional Operation Using Native Mode

Bidirectional operation for valid I/O standards is fully supported using the native mode primitives described earlier in this chapter. In native mode, BITSLICE_CONTROL is used with both the RX_BITSLICE and TX_BITSLICE primitives, as shown in Figure 2-17. Only one bidirectional I/O is shown for clarity.

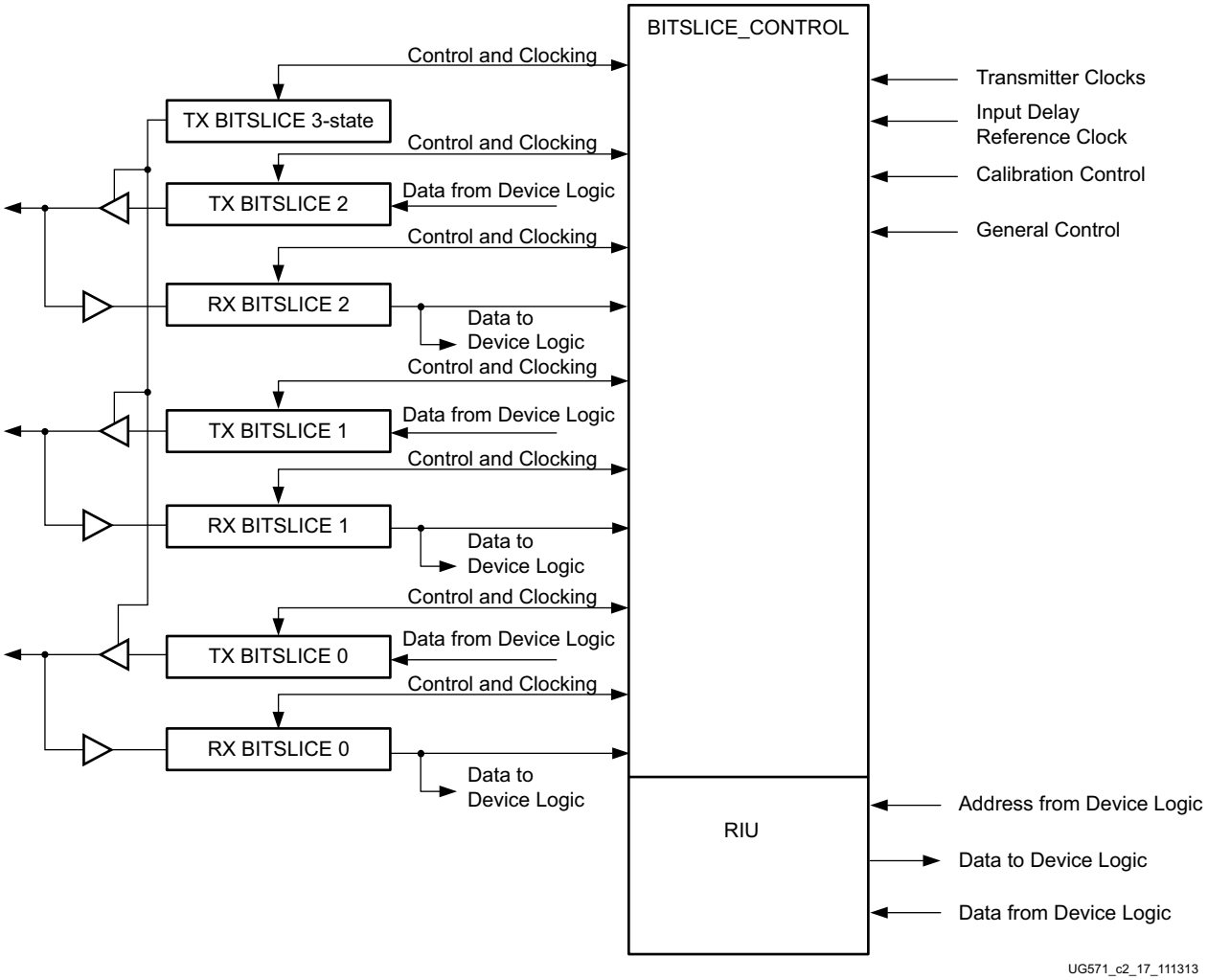

Figure 2-17: **Bidirectional Operation Using Native Mode**

Termination Options for Simultaneous Switching Noise Analysis

Termination Options

The Vivado® Design Suite can perform simultaneous switching noise (SSN) analysis for each design, taking into account the actual I/O standards and options assigned to the I/O pins in the target device and package.

For each output pin, there is the option to specify whether or not termination is present on the board. The off-chip termination field automatically populates with the default terminations for each I/O standard, if one exists.

Table A-1 lists all of the default terminations for each of the I/O standards supported by UltraScale devices when using the SSN predictor tool within the Vivado Design Suite. For each I/O pin in the design, you can specify whether to use these terminations, or to have no termination.

Table A-1: **Default Terminations for SSN Noise Analysis by I/O Standard**

I/O Standard	Drive	Termination Option
BLVDS_25	–	Near Series 165Ω, Near Differential 140Ω, and Far Differential 100Ω
DIFF_HSTL_I	–	Far V_{TT} 40Ω
DIFF_HSTL_I_12	–	Far V_{TT} 40Ω
DIFF_HSTL_I_DCI_12	–	Far V_{TT} 40Ω
DIFF_HSTL_I_18	–	Far V_{TT} 50Ω
DIFF_HSTL_I_DCI	–	Far V_{TT} 40Ω
DIFF_HSTL_I_DCI_18	–	Far V_{TT} 50Ω
DIFF_HSTL_II	–	Near V_{TT} 50Ω & Far V_{TT} 50Ω
DIFF_HSTL_II_18	–	Near V_{TT} 50Ω & Far V_{TT} 50Ω
DIFF_HSUL_12	–	None
DIFF_HSUL_12_DCI	–	None
DIFF_POD10	–	Far V_{CCO} 40Ω
DIFF_POD10_DCI	–	Far V_{CCO} 40Ω

Table A-1: **Default Terminations for SSN Noise Analysis by I/O Standard *(Cont'd)***

I/O Standard	Drive	Termination Option
DIFF_POD12	–	Far V_{CCO} 40Ω
DIFF_POD12_DCI	–	Far V_{CCO} 40Ω
DIFF_SSTL12	–	Far V_{TT} 40Ω
DIFF_SSTL12_DCI	–	Far V_{TT} 40Ω
DIFF_SSTL135	–	Far V_{TT} 40Ω
DIFF_SSTL135_DCI	–	Far V_{TT} 40Ω
DIFF_SSTL135_R	–	Far V_{TT} 40Ω
DIFF_SSTL15	–	Far V_{TT} 40Ω
DIFF_SSTL15_DCI	–	Far V_{TT} 40Ω
DIFF_SSTL15_R	–	Far V_{TT} 50Ω
DIFF_SSTL18_I	–	Far V_{TT} 50Ω
DIFF_SSTL18_I_DCI	–	Far V_{TT} 50Ω
DIFF_SSTL18_II	–	Near V_{TT} 50Ω & Far V_{TT} 50Ω
HSLVDCI_15	–	None
HSLVDCI_18	–	None
HSTL_I	–	Far V_{TT} 40Ω
HSTL_I_12	–	Far V_{TT} 40Ω
HSTL_I_DCI_12	–	Far V_{TT} 40Ω
HSTL_I_18	–	Far V_{TT} 50Ω
HSTL_I_DCI	–	Far V_{TT} 40Ω
HSTL_I_DCI_18	–	Far V_{TT} 50Ω
HSTL_II	–	Near V_{TT} 50Ω & Far V_{TT} 50Ω
HSTL_II_18	–	Near V_{TT} 50Ω & Far V_{TT} 50Ω
HSUL_12	–	None
HSUL_12_DCI	–	None
LVCMOS12	2	None
LVCMOS12	4	None
LVCMOS12	6	None
LVCMOS12	8	None
LVCMOS12	12	Far V_{TT} 50Ω
LVCMOS15	2	None
LVCMOS15	4	None
LVCMOS15	6	None
LVCMOS15	8	None
LVCMOS15	12	Far V_{TT} 50Ω

Table A-1: **Default Terminations for SSN Noise Analysis by I/O Standard *(Cont'd)***

I/O Standard	Drive	Termination Option
LVCMOS15	16	Far V_{TT} 50Ω
LVCMOS18	2	None
LVCMOS18	4	None
LVCMOS18	6	None
LVCMOS18	8	None
LVCMOS18	12	Far V_{TT} 50Ω
LVCMOS18	16	Far V_{TT} 50Ω
LVCMOS25	4	None
LVCMOS25	8	None
LVCMOS25	12	Far V_{TT} 50Ω
LVCMOS25	16	Far V_{TT} 50Ω
LVCMOS33	4	None
LVCMOS33	8	None
LVCMOS33	12	Far V_{TT} 50Ω
LVCMOS33	16	Far V_{TT} 50Ω
LVDCI_15	–	None
LVDCI_18	–	None
LVDS	–	Far Differential 100Ω
LVDS_25	–	Far Differential 100Ω
LVDS_25_PE	–	Far Differential 100Ω
LVDS_PE	–	Far Differential 100Ω
LVTTL	4	None
LVTTL	8	None
LVTTL	12	Far V_{TT} 50Ω
LVTTL	16	Far V_{TT} 50Ω
MINI_LVDS_25	–	Far Differential 100Ω
POD10	–	Far V_{CCO} 40Ω
POD10_DCI	–	Far V_{CCO} 40Ω
POD12	–	Far V_{CCO} 40Ω
POD12_DCI	–	Far V_{CCO} 40Ω
PPDS_25	–	Far Differential 100Ω
RSDS_25	–	Far Differential 100Ω
SSTL12	–	Far V_{TT} 40Ω
SSTL12_DCI	–	Far V_{TT} 40Ω
SSTL135	–	Far V_{TT} 40Ω

Table A-1: **Default Terminations for SSN Noise Analysis by I/O Standard *(Cont'd)***

I/O Standard	Drive	Termination Option
SSTL135_DCI	–	Far V_{TT} 40Ω
SSTL135_R	–	Far V_{TT} 40Ω
SSTL15	–	Far V_{TT} 40Ω
SSTL15_DCI	–	Far V_{TT} 40Ω
SSTL15_R	–	Far V_{TT} 50Ω
SSTL18_I	–	Far V_{TT} 50Ω
SSTL18_I_DCI	–	Far V_{TT} 50Ω
SSTL18_II	–	Near V_{TT} 50Ω & Far V_{TT} 50Ω
TMDS_33	–	Far 3.3V 50Ω
SUB_LVDS	–	Far Differential 100Ω

Figure A-1 illustrates each of these terminations.

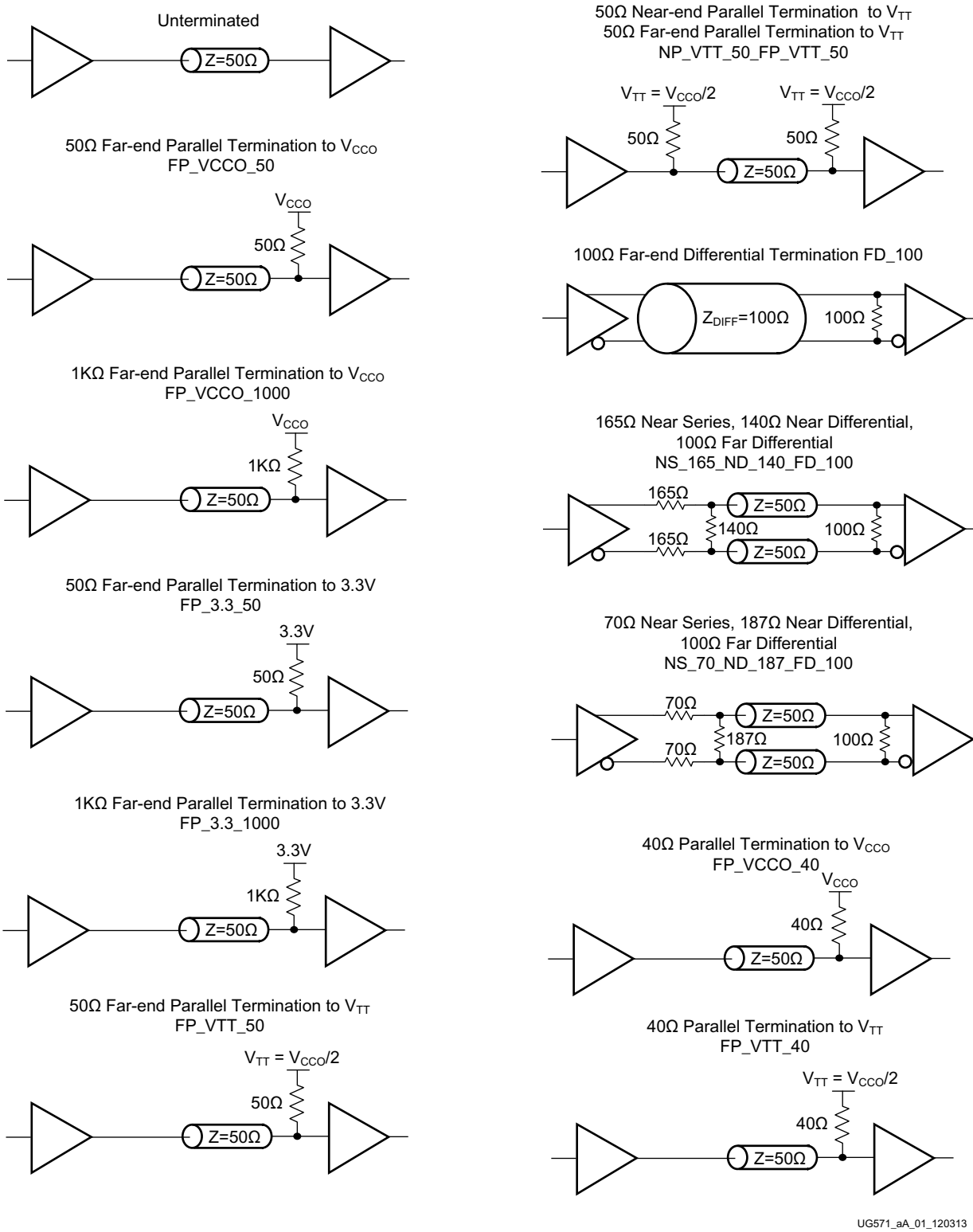

Figure A-1: **Default Terminations**

Appendix B

Additional Resources and Legal Notices

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see Xilinx Support.

For a glossary of technical terms used in Xilinx documentation, see the Xilinx Glossary.

Solution Centers

See the Xilinx Solution Centers for support on devices, software tools, and intellectual property at all stages of the design cycle. Topics include design assistance, advisories, and troubleshooting tips.

References

These documents and links provide supplemental material useful with this guide:

1. UltraScale device data sheets:
   - *Kintex UltraScale Architecture Data Sheet: DC and AC Switching Characteristics* (DS892)
   - *Virtex UltraScale Architecture Data Sheet: DC and AC Switching Characteristics* (DS893)
2. *UltraScale Architecture and Product Overview* (DS890)
3. *UltraScale Architecture Packaging and Pinout Specifications* (UG575)
4. *UltraFast Design Methodology Guide for the Vivado Design Suite* (UG949)
5. *Vivado Design Suite User Guide: System-Level Design Entry* (UG895)
6. *UltraScale Architecture Libraries Guide* (UG974)
7. *Vivado Design Suite Properties Reference Guide* (UG912)

8. Electronic Industry Alliance JEDEC web site at www.jedec.org
9. *UltraScale Architecture Clocking Resource User Guide* (UG572)

Please Read: Important Legal Notices