Use ZCU102 TRD to Accelerate Development of ZYNQ UltraScale+ MPSoC
Topics

- Hardware advantages of ZYNQ UltraScale+ MPSoC
- Software stacks of MPSoC
- Target reference design introduction
- Details about one Design Modules (DM) in ZCU102 TRD
Hardware Advantages of MPSoC
Zynq UltraScale+ MPSoC

ARM Cortex® R5
Real-Time Processors
32-bit Dual-Core

ARM Cortex® A53
Application Processor
64-bit Dual/Quad-Core

Fabric Acceleration
Customizable Engines
High Speed Connectivity

Memory Subsystem
High Bandwidth
Low Latency

Graphics Processor
ARM Mali-400MP2

Platform & Power Management
Granular Power Control
Functional Safety

Configuration & Security Unit
Anti-Tamper & Trust
Industry Standards

Video Codec
H.265 HEVC
Video Codec
8K4K (15fps)
4K2K (60fps)

High Speed Peripherals
Key Interfaces

Quad-Core ARM® Cortex™-A53
Dual-Core ARM® Cortex™-R5
Memory Subsystem
ARM Mali-400MP2
Platform Management Unit
Config and Security
System Functions
DisplayPort
USB 3.1
SATA
PCIe® Gen3
GigE
CAN
SD/MMC
NAND

UltraRAM
100G Ethernet
150G Interlaken

16G & 33G Transceivers
PCle® Gen4

Graphics Processor
ARM Mali
ARM Mali-400MP2

High Speed Connectivity
Video Codec
8K4K (15fps)
4K2K (60fps)
64-bit increases compute capability with 32-bit compatibility

2.7X performance/watt (DMIPS) vs. predecessor

SIMD engine accelerates multimedia, signal & image processing

Deterministic processing for critical real-time operation

Split-Mode, and Lock-Step Mode for fault tolerance & detection

256KB TCM for deterministic and low-latency response

32GB of Addressable Memory. 2400Mbps for DDR4 & LPDDR4

6 AXI Ports for high memory bandwidth

256KB low latency OCM w/ECC, no need for external memory
Zynq UltraScale+ MPSoC

- ACE bi-directional port for coherent memory access between a coherent master & A53 (CCI)
- HPC ports for coherent memory access between a DMA and A53
- Twelve 128-bit AXI ports, 6,000 interconnects between PS & PL

- H.264 and H.265 standards
- Up to a 4K x 2K@60/8K x 4K@15 Hz rate, 8-bit and 10-bit color depth, YCbCr 4:2:2 and 4:2:0 video formats
- Low-latency mode

- Most power-optimized ARM GPU with Full HD support (1080p)
- Ideal for 2D vector graphics and 3D graphics
- Supports open standards, e.g., OpenGL ES 1.1 & 2.0
Zynq UltraScale+ MPSoC

High Speed Peripherals
Key Interfaces
- 6G Transceivers supports PCIe, DisplayPort, SGMII, SATA, USB 3.0
- DisplayPort up to 4K x 2K @ 30fps, with alpha blending
- Gigabit Ethernet, SD/SDIO, Quad-SPI, SPI, NAND, CAN, UART, I2C, USB 2.0

Configuration & Security Unit
Anti-Tamper & Trust Industry Standards
- Boot from Quad SPI Flash, NAND Flash, SD 3.0, or eMMC
- Fault tolerant device boot: secure and non-secure
- Dedicated decryption (AES-256) & authentication (4096-bit RSA key, SHA3 hash functions) engines

Platform & Power Management
Granular Power Control Functional Safety
- Granular architecture enabling block-level power management
- Eliminate static power of unused blocks
- Enables extensible runtime power management (RAM)
More than Just Silicon

- Run-Time Software
- System Software
- Design Tools
- Reference Designs
- Emulation & Development Kits
- Rapid Development
Zynq MPSoC Toolflow

Hardware

- Configure Processing System
- Add IP
- Add custom RTL*
- Implementation
- Simulation*
- Generate Bitstream

Software

- Hardware Handoff File (HDF)
- Hardware Handoff Module (HSM)

- PetaLinux
  - Extract Platform
  - Configure Kernel/System
  - Configure the Kernel
  - Build Kernel/File System
  - Generate Linux System

- Create BSP
- Integrate OS
- Add PMU Firmware*
- Add XEN/ATF*
- Generate FSBL
- Write Applications
- Debug, Profiling, Performance Modeling*
- Create Boot Image

* optional step
Embedded Software Development Tools

<table>
<thead>
<tr>
<th>Feature</th>
<th>Benefit</th>
</tr>
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<tbody>
<tr>
<td>Eclipse-Based IDE</td>
<td>Familiar SW development environment – Xilinx Software Design Kit (SDK)</td>
</tr>
<tr>
<td>Linaro GCC Tool Chain</td>
<td>Industry standard compiler tool chain for Embedded Linux &amp; Bare Metal</td>
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<tr>
<td>Multi-Core Debug</td>
<td>Debug &amp; cross triggering for Cortex-A53s, Cortex-R5s, and MicroBlaze™ Processor</td>
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<tr>
<td>Performance Profiling &amp; Analysis</td>
<td>Analyze interfaces across processing and programmable logic domains</td>
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| Ecosystem Development Tools    | • Broad support for 3rd party dev tools & debug, e.g., ARM DS-5, Lauterbach Trace-32  
                                | • Designers use their preferred development & debug environment          |
PetaLinux

➢ PetaLinux is a build tool that allows end users to quickly bring up embedded Linux systems

➢ Why PetaLinux?
  – Simplifies the Linux configuration and build system for Xilinx SoC FPGA
  – Automatically configure Linux kernel, U-Boot, root file system, and application(s) to target a particular Vivado project
  – Four commands to boot up embedded Linux for Xilinx SoC FPGA
Typical use case: APU SMP & AMP

**SMP Linux on Cortex-A53**
- No Hypervisor needed
- Linux Application and interrupt handler can be bound to a specific core

**AMP on Cortex-A53**
- Hypervisor is needed
- Easy legacy system migration
Typical use case: RPU

**Split mode (default)**
- R5-0: FreeRTOS
- R5-1: BareMetal or other RTOS

**Lockstep mode**
- R5-0/R5-1: FreeRTOS
- Continually comparing outputs running the same software
OpenAMP provides software components to enable development of software applications for APU + RPU systems.

- Remoteproc: controls the Life Cycle Management (LCM) of the remote processors from the master processor.
- RPMmsg API: allows Inter Process Communications (IPC) between software running on independent cores in an AMP system.
# System Software

## Out-of-the-Box Firmware, Drivers, Frameworks

<table>
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<td>First Stage Boot Loader (FSBL)</td>
<td>Generated from the Hardware Handoff (HDF) file</td>
</tr>
<tr>
<td>Power Management Framework</td>
<td>Standard APIs for power management</td>
</tr>
<tr>
<td>ARM® Trusted Firmware</td>
<td>OpenSource firmware to boot secure OS, leverage ARMv8-A virtualization features</td>
</tr>
<tr>
<td>U-Boot</td>
<td>Out-of-the-box boot loaders</td>
</tr>
<tr>
<td>Linux Kernel</td>
<td>Standard Linux Kernel from mainline</td>
</tr>
<tr>
<td>Inter-Processor Framework (OpenAMP)</td>
<td>Framework for inter-OS &amp; inter-processor management &amp; communication (APU &amp; RPU)</td>
</tr>
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**Diagram:**

- Processing System
  - APU
  - Memory
  - GPU
  - Peripherals
  - Inter-Processor Framework
  - Security Firmware
  - RPU
  - CSU
  - PMU
  - System Control
SDSoC accelerate SW to HW

- Convert software algorithm to hardware design
- Automatically generate data mover network
- Explore different architecture to find the optimal
Targeted Reference Design
What is TRD
- Design enables customers to evaluate the Zynq UltraScale+ MPSoC
- Provides demonstration of Zynq UltraScale+ MPSoC features
- Provides a starting platform upon which users may implement their own designs
- Design provides a ready to run demonstration enabling a positive out-of-box experience

Design is delivered as a standard TRD with associated documentation
- Design Details: UG1221: Zynq UltraScale+ MPSoC Base Targeted Reference Design

Design Demonstrates
- APU Running SMP Linux
- RPU-1 Running Bare Metal
- RPU-0 Running FreeRTOS
- Basic 4K video pipe controlled by the Processing System
- Multiple choices of video source and sink

Reference Design Conception
- Divide a complex design into multiple design modules (DM) to help to understand each part
- Each DM can be verified separately
Hardware Interfaces & IP

GPU

Video Inputs
- TPG
- USB Webcam (optional)
- Vivid (Virtual video device)
- HDMI (2017.1)

Video Outputs
- DisplayPort Tx
- HDMI (2017.1)

Video Processing
- 2D Convolution Filter
- Optical Flow (2017.1)

Auxiliary Peripherals
- SD
- I2C
- GPIO
- Ethernet
- UART
- USB 2.0 / 3.0
- APM
- SATA (2017.1)
Software Components

▷ Operating systems
  – APU: SMP Linux
  – RPU-0: FreeRTOS
  – RPU-1: Bare-metal

▷ Linux frameworks/libraries
  – Video: Video4Linux (V4L2), Media Controller
  – Display: DRM/KMS, X-Server (X.Org)
  – Graphics: Qt5, OpenGL ES2
  – Vision: OpenCV
  – Inter-process communication: OpenAMP

▷ User applications
  – APU: Video control application with GUI
  – RPU-0: Multi-threaded heartbeat application
    • FreeRTOS
  – RPU-1: Performance monitoring application
    • Bare-metal
Video Pipeline Block Diagram
DM1: APU SMP Linux
Block Diagram and DM(2)

DM1: APU SMP Linux
DM2: RPU0 FreeRTOS Application
Block Diagram and DM(3)

DM1: APU SMP Linux
DM2: RPU0 FreeRTOS Application
DM3: RPU1 Bare-metal Application
Block Diagram and DM(4)

DM1: APU SMP Linux
DM2: RPU0 FreeRTOS Application
DM3: RPU1 Bare-metal Application
DM4: APU/RPU1 Inter Process Communication
DM1: APU SMP Linux
DM2: RPU0 FreeRTOS Application
DM3: RPU1 Bare-metal Application
DM4: APU/RPU1 Inter Process Communication
DM5: APU Qt Application
Demo GUI

Video Info Panel

System Performance Panels

Control Bar
Block Diagram and DM(6)

DM6: PL Video Capture
Block Diagram and DM(7)

DM6: PL Video Capture
DM7: OpenCV-based Image Processing
Block Diagram and DM(8)

DM6: PL Video Capture
DM7: OpenCV-based Image Processing
DM8: PL-accelerated Image Processing
Block Diagram and DM(9)

DM6: PL Video Capture
DM7: OpenCV-based Image Processing
DM8: PL-accelerated Image Processing
DM9: Two Image Processing Functions
Hardware Platform and Connectivity Overview
Boot Flow
DM Highlights

- DM1 – APU SMP Linux
- DM2 – RPU0 FreeRTOS Application
- DM3 – RPU1 Bare-metal Application
- DM4 – APU/RPU1 Inter Process Communication
- DM5 – APU Qt Application
- DM6 – PL Video Capture
- DM7 – OpenCV-based Image Processing
- DM8 – PL-accelerated Image Processing
- DM9 – Two Image Processing Functions
- DM10 – Full-fledged Base TRD
DM4: APU/RPU Inter-processor Communication
OpenAMP provides software components to enable development of software applications for APU + RPU systems.

- Remoteproc: controls the Life Cycle Management (LCM) of the remote processors from the master processor.
- RPMsg API: allows Inter Process Communications (IPC) between software running on independent cores in an AMP system.
AMP System Terminology

- A master is defined as the CPU that is booted first.
- A remote is defined as a CPU managed by a master CPU.
- The master CPU brings up and takes down the remote CPU.
- The master communicates with the remote to offload work.
- The master and remote CPUs may be homogeneous or heterogeneous.
- The master/remote roles are typically static at build time.
Master Remoteproc APIs

The *remoteproc* APIs provides four functions for the master CPU

1. Load the code and data of the remote CPU into memory
2. Start the remote CPU with reset and clock control
3. Manage a communication channel with the remote CPU
4. Shut down the remote CPU with reset and clock control
Remote Remoteproc APIs

> The *remoteproc* APIs also support the remote CPU
> It provides three functions for the remote CPU

1. Initialization of the remoteproc system on the remote CPU
2. Manage a communication channel with the master CPU
3. Shutdown of the remoteproc system on the remote CPU
Remote Processor (remoteproc) Component

▷ The remote firmware includes a statically linked resource table
▷ The resource table describes the required system resources
▷ The firmware is parsed by the master to get the resource table

Examples of resources in the resource table include:
- memory regions (carve-outs) for code and data sections
- memory regions to describe interprocessor communication
rpmsg is a messaging bus to allow communication between CPUs
Each CPU is device on the messaging bus
A channel is a communication link between CPUs on the bus
A channel is created when the remote CPU is started
A channel is identified by a name together with source and destination addresses
The **virtio** component is used to implement **rpmsg**

It provides virtual I/O services to support communication between the master and remote

A **vring** is a transport abstraction for I/O operations used by virtio

A **vring** implements a ring buffer
The firmware build consists of multiple libraries which are combined with the application.

The resource table is built into the application.

The resource table is linked into a section the master knows how to find it in the application.

Each library is built based on the role (master or remote).
OpenAMP Documents

- **OpenAMP Wiki**

- **Github Repository**
  - [https://github.com/OpenAMP/open-amp](https://github.com/OpenAMP/open-amp)

- **OpenAMP Get Start Guide**

- **ZCU102 TRD Document**
  - UG1221
Wrap up
Summary

» Heterogeneous Multi-Processing SoC Hardware
  – Quad core ARM Cortex-A53
  – Dual core ARM Cortex-R5
  – Multiple acceleration engines and high speed peripherals
  – Programmable Logic

» Complete Software Stacks
  – SMP Linux
  – AMP and Inter-Processor Communication
  – SDSoC for accelerator design with C

» Targeted Reference Design
  – Make good use of MPSoC architecture
  – Good reference for start
Support

» Known issues and limitations

» Discussion
  – [Xilinx Community Forums](https://community.xilinx.com)
  – Please include "ZCU102 Base TRD" and the release version in the topic
Explore More in xilinx.com

» ZCU102 TRD, example designs, documents and board files
   – https://www.xilinx.com/zcu102

» reVision
   – https://www.xilinx.com/revision

» Open source Linux documents and tips at http://wiki.xilinx.com
   – MPSoC Ubuntu Desktop: http://www.wiki.xilinx.com/+Zynq+UltraScale%EF%BC%8B+MPSoC+Ubuntu+Desktop
   – PetaLinux Yocto Tips: http://www.wiki.xilinx.com/PetaLinux+Yocto+Tips

» Known Issue Answer Records
   – https://www.xilinx.com/support.html#knowledgebase
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