XUPV5-LX110T PCIe x1 Endpoint Plus Design Creation

Using ISE™ 10.1i SP3, Core generator 10.1i SP3

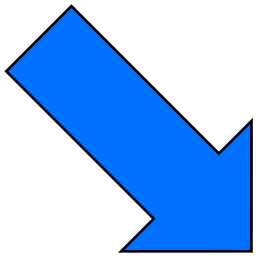
September, 2008

XUPV5-LX110T PCIe Overview

- Software Requirements
- Hardware Setup
- Design Creation
  - Highlighting the Virtex-5 RocketIO™ GTP/GTX Transceivers
- Testing the design

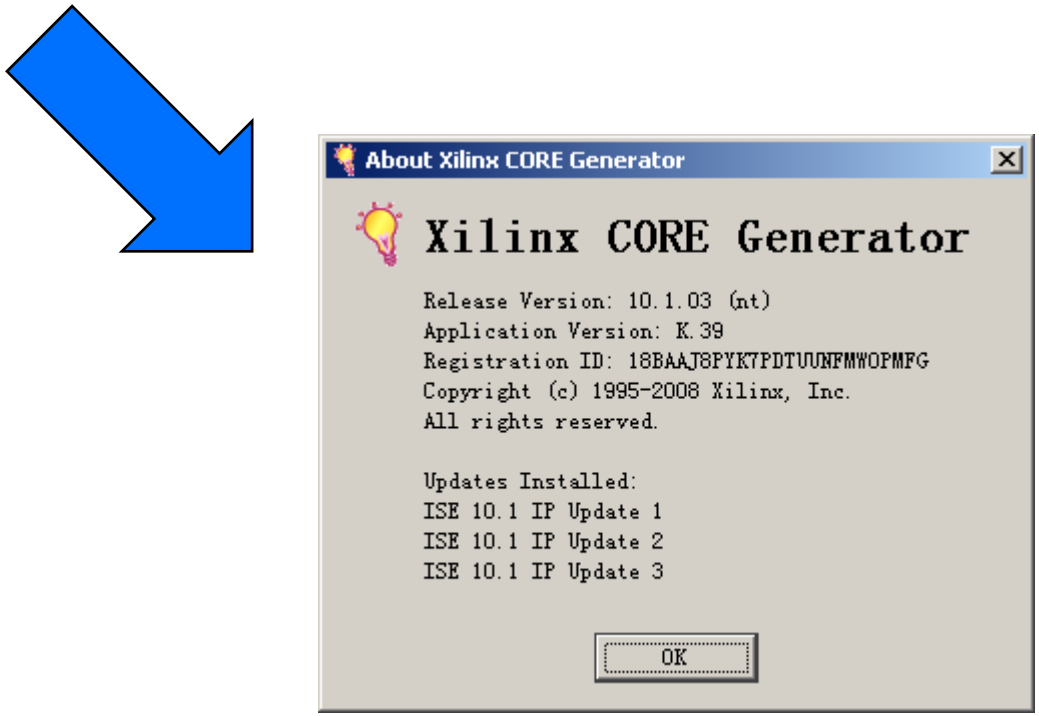
ISE Software Requirement

- Xilinx ISE 10.1i SP3 software



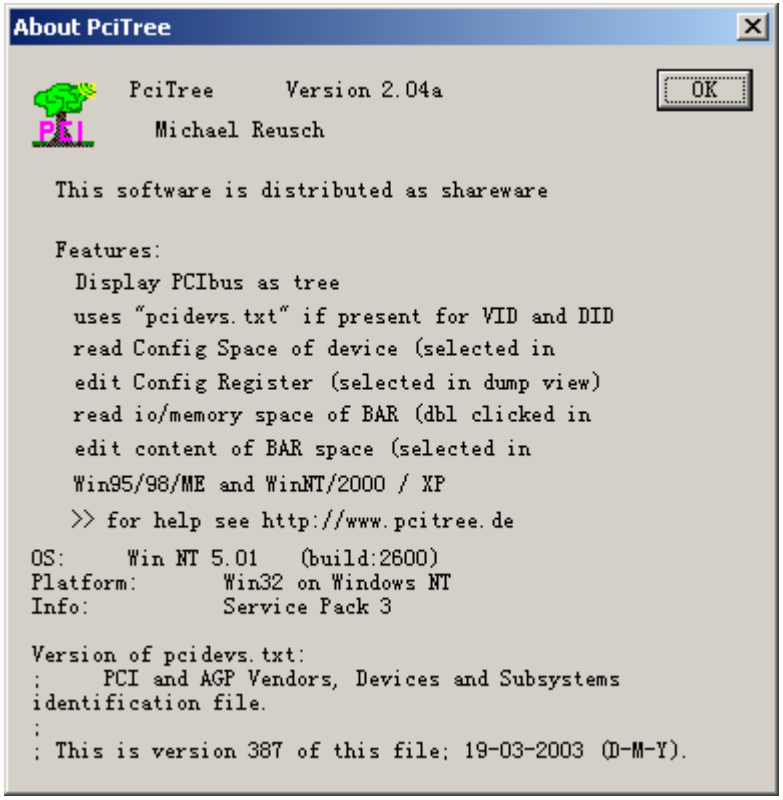
Coregen Software Requirement

- Install Xilinx Coregen 10.1i IP Update 3

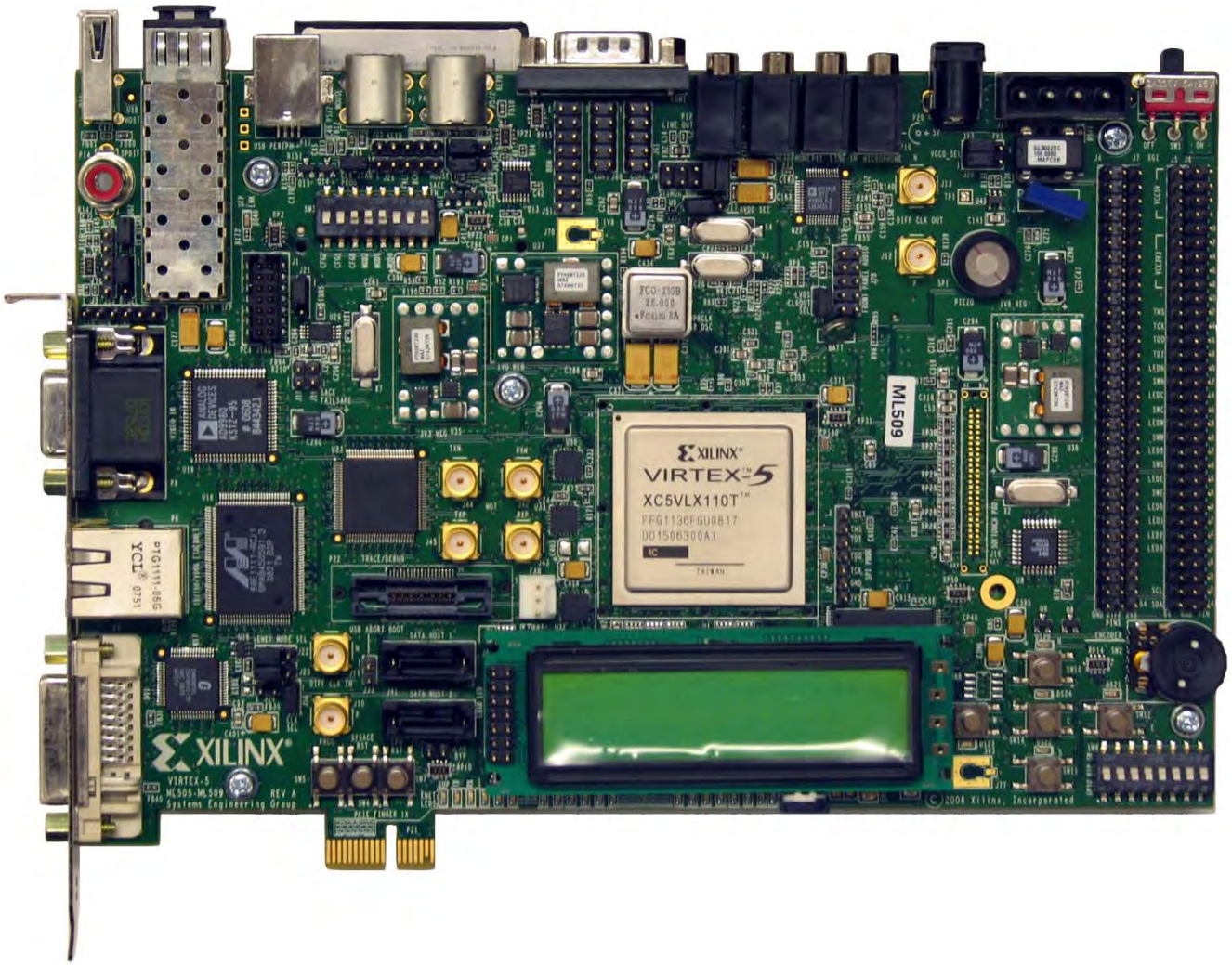


Software Requirement

- PciTree Bus Viewer
  - Free download from http://www.pcitree.de/index.html
  - HLP.SYS must be copied to C:\WINDOWS\system32\drivers directory



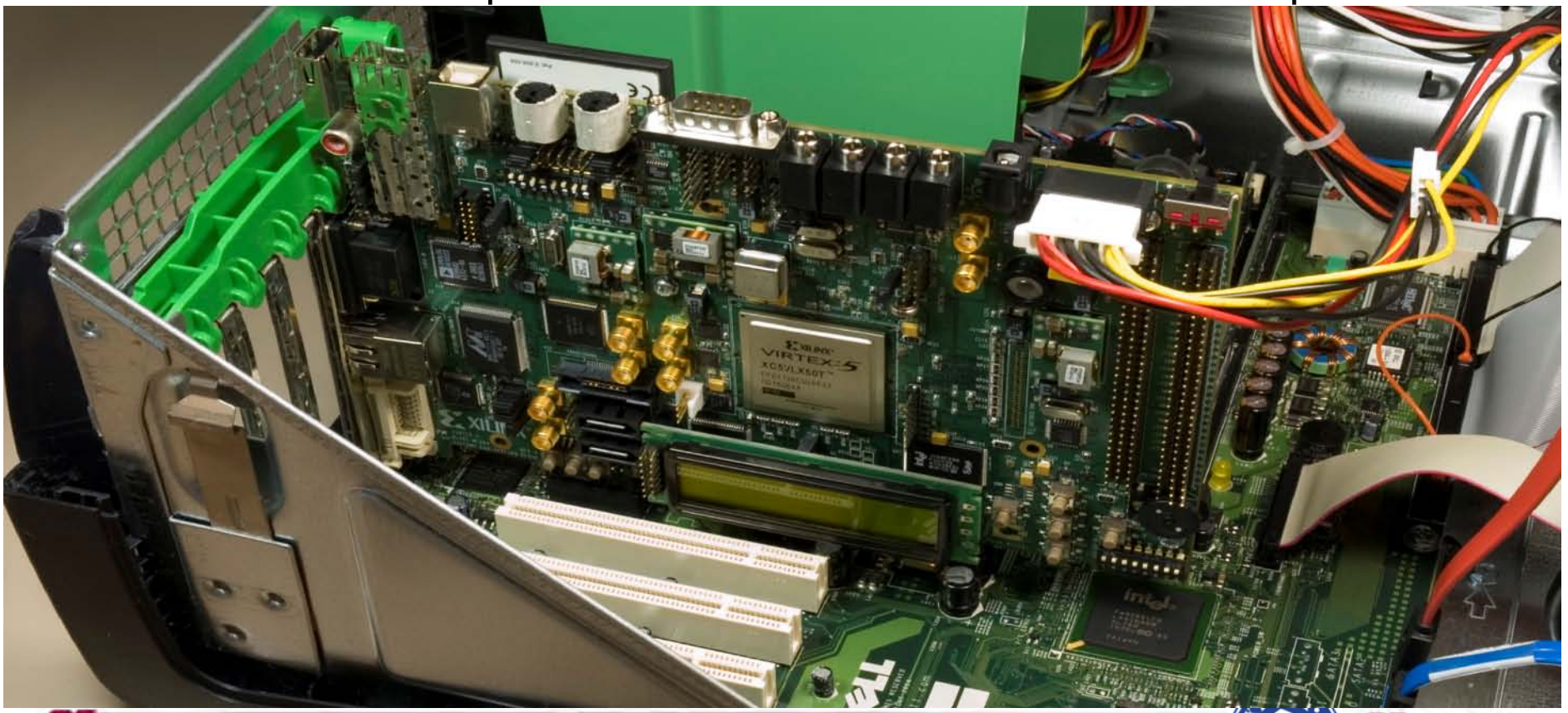
Xilinx XUPV5-LX110T Board



Note: The XUPV5-LX110T uses an XC5VLX110T FPGA.

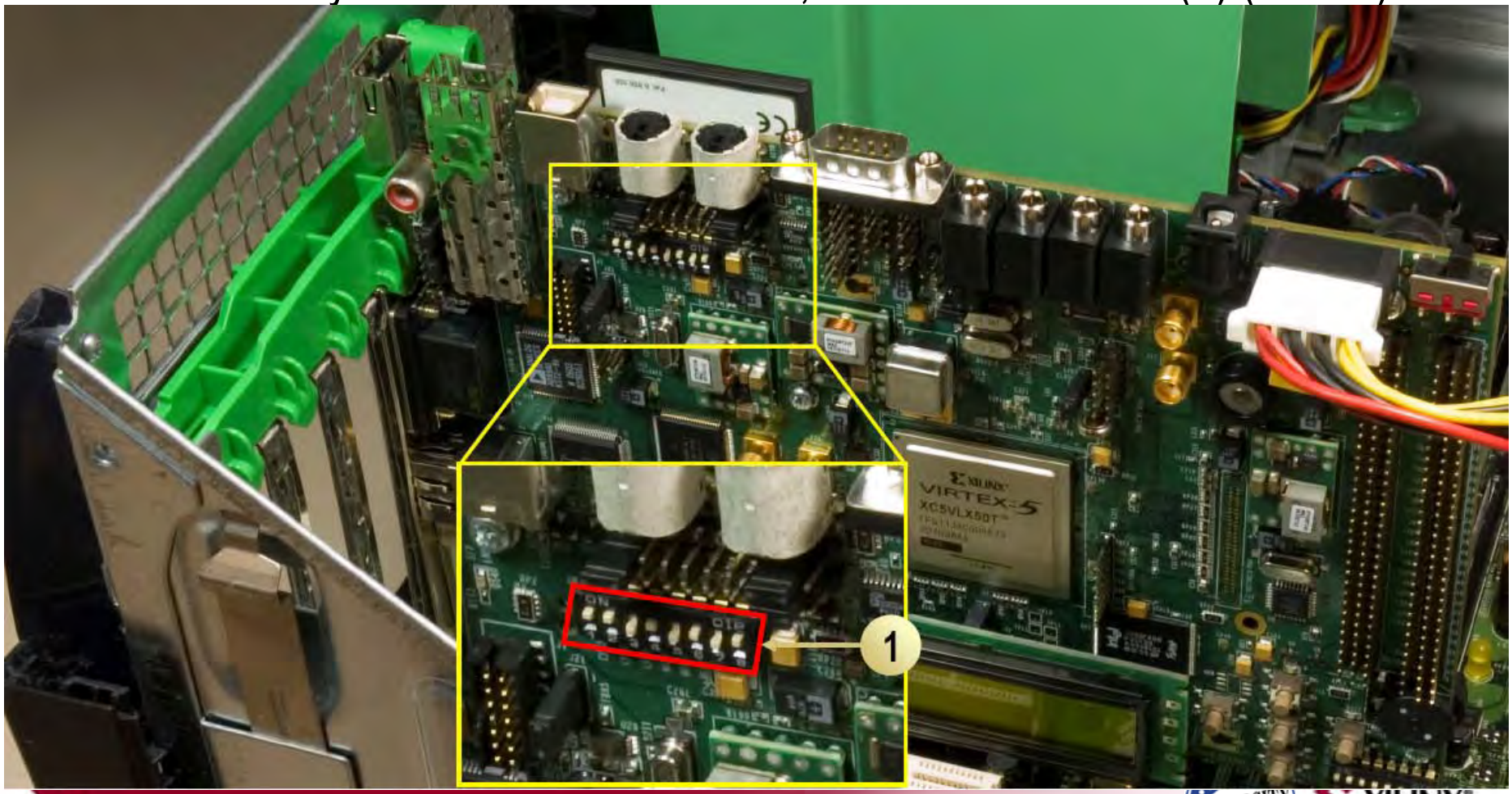
Setting Up the Hardware

- Insert the XUPV5-LX110T Board into a PCIe x1 slot
  - Connect PC power or use XUPV5-LX110T Power Adapter



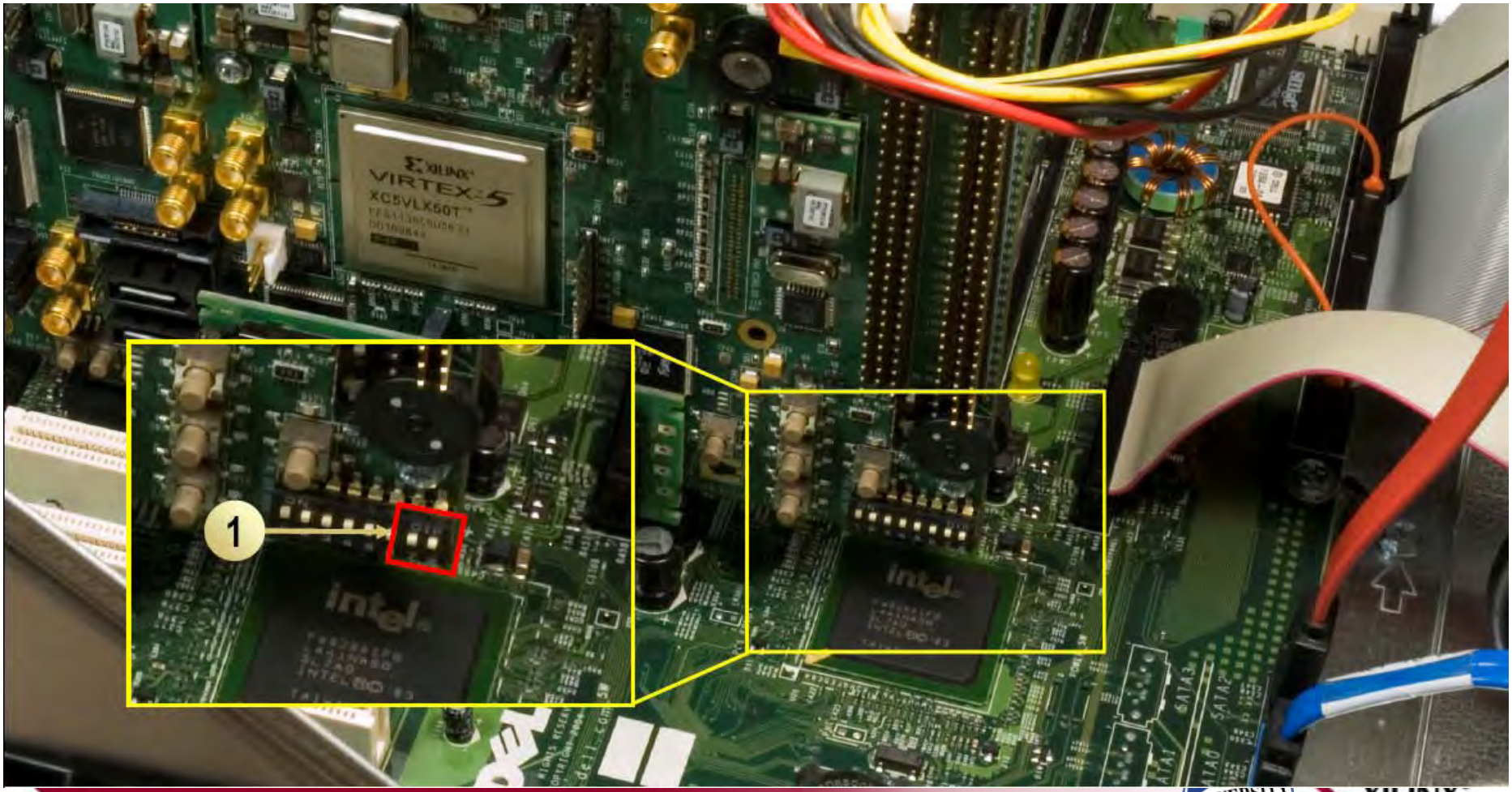
Setting Up the Hardware

- Set the System ACE DIP switches, SW3 to 11010101 (1) (1 = on)



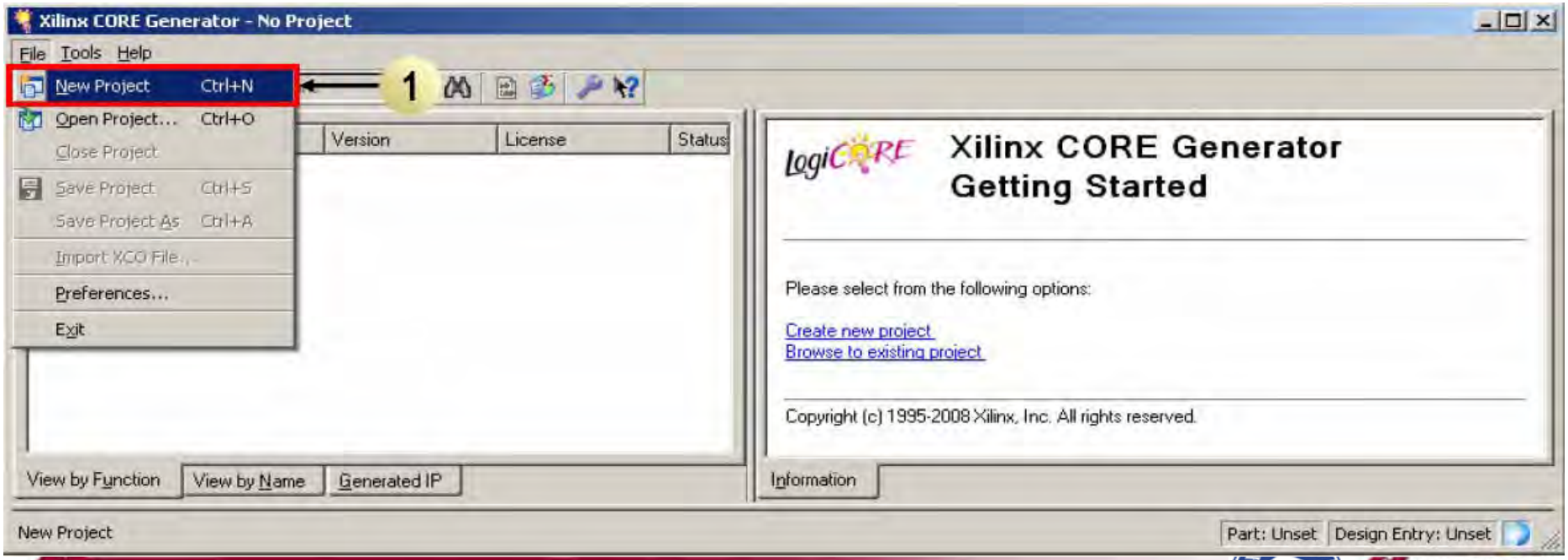
Setting Up the Hardware

- Set DIP Switch SW8, bit 7 & 8 to up as per AR24826



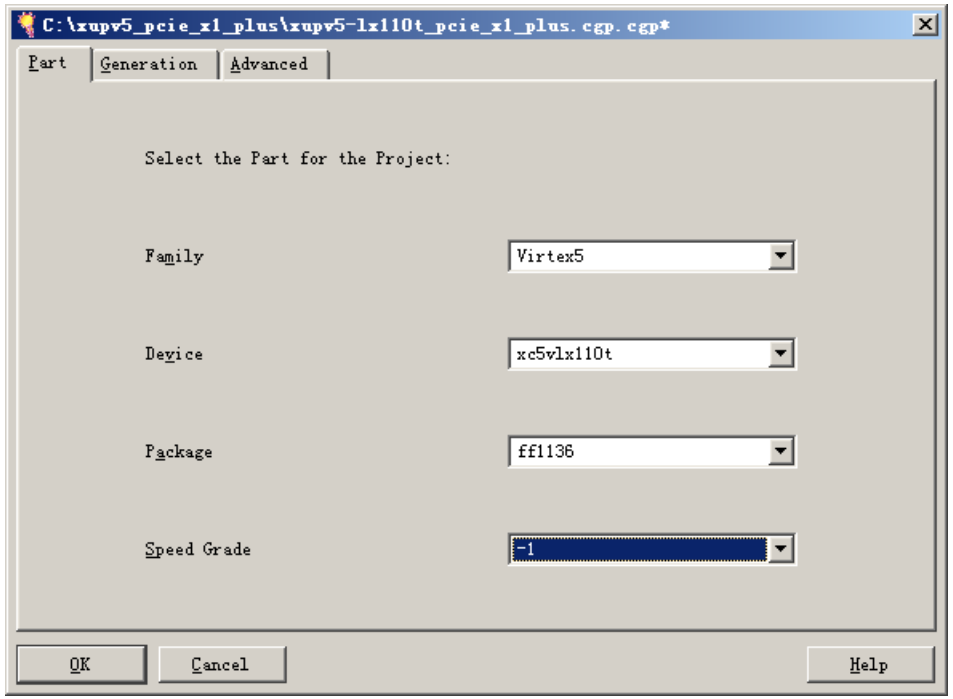
CORE Generator

- Open the CORE Generator
  - Start → All Programs → Xilinx ISE Design Suite 10.1i → ISE → Accessories → CORE Generator
- Create a new project; select File → New Project (1)



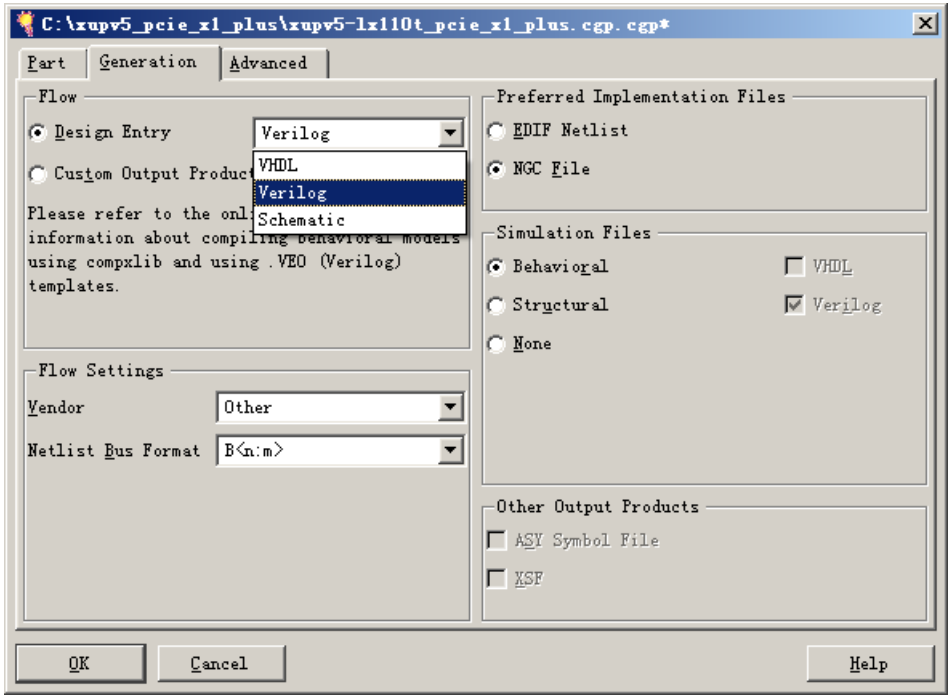
PCIe Core Generation

- Create a project directory: xupv5_pcie_x1_plus
- Name the project: xupv5-lx110t_pcie_x1_plus.cgp
- Set the Part:
  - Family: Virtex5
  - Device: xc5vlx110t
  - Package: ff1136
  - Speed Grade: -1



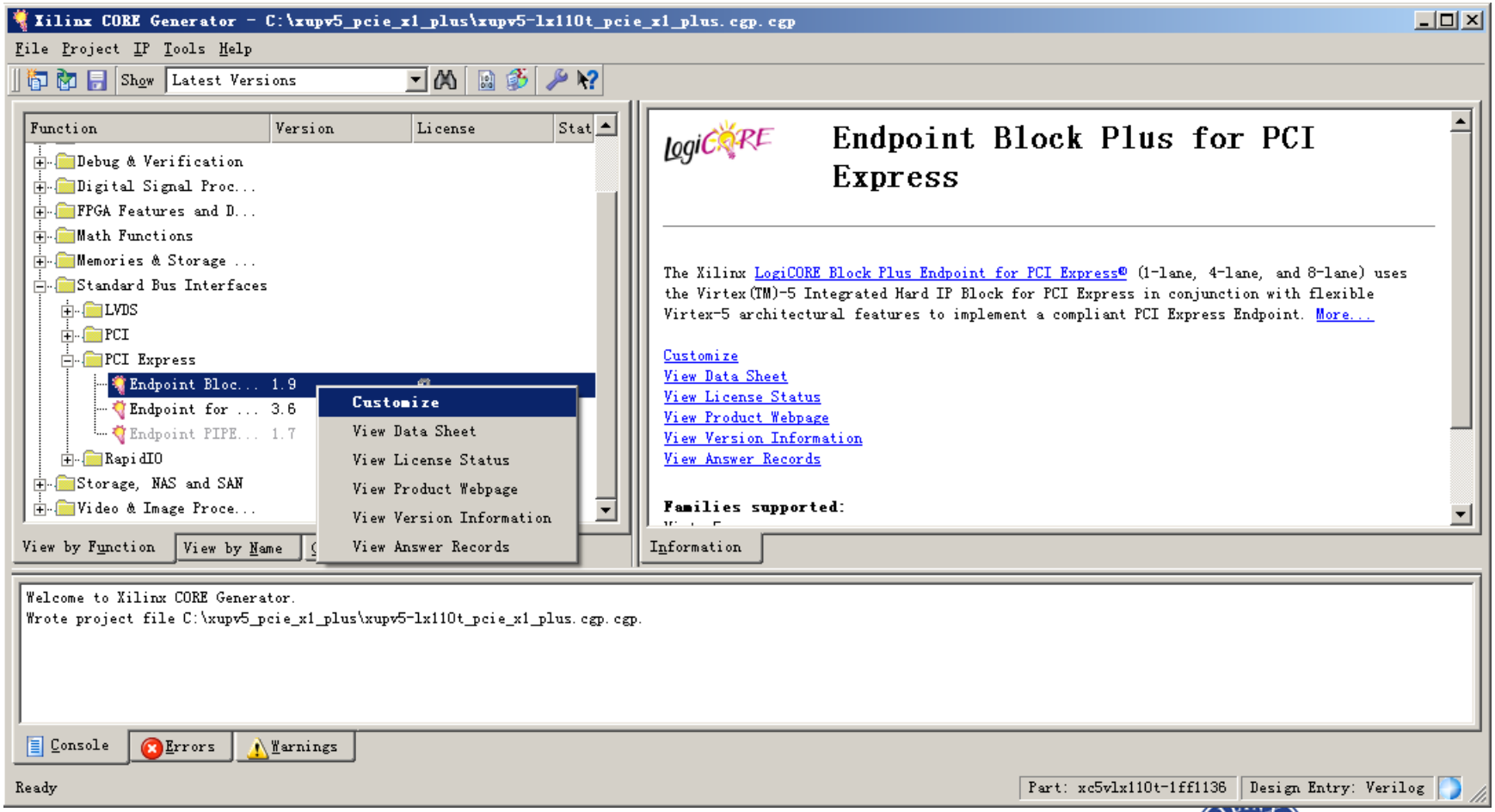
PCIe Core Generation

- Set the Design Entry to Verilog
- Click OK



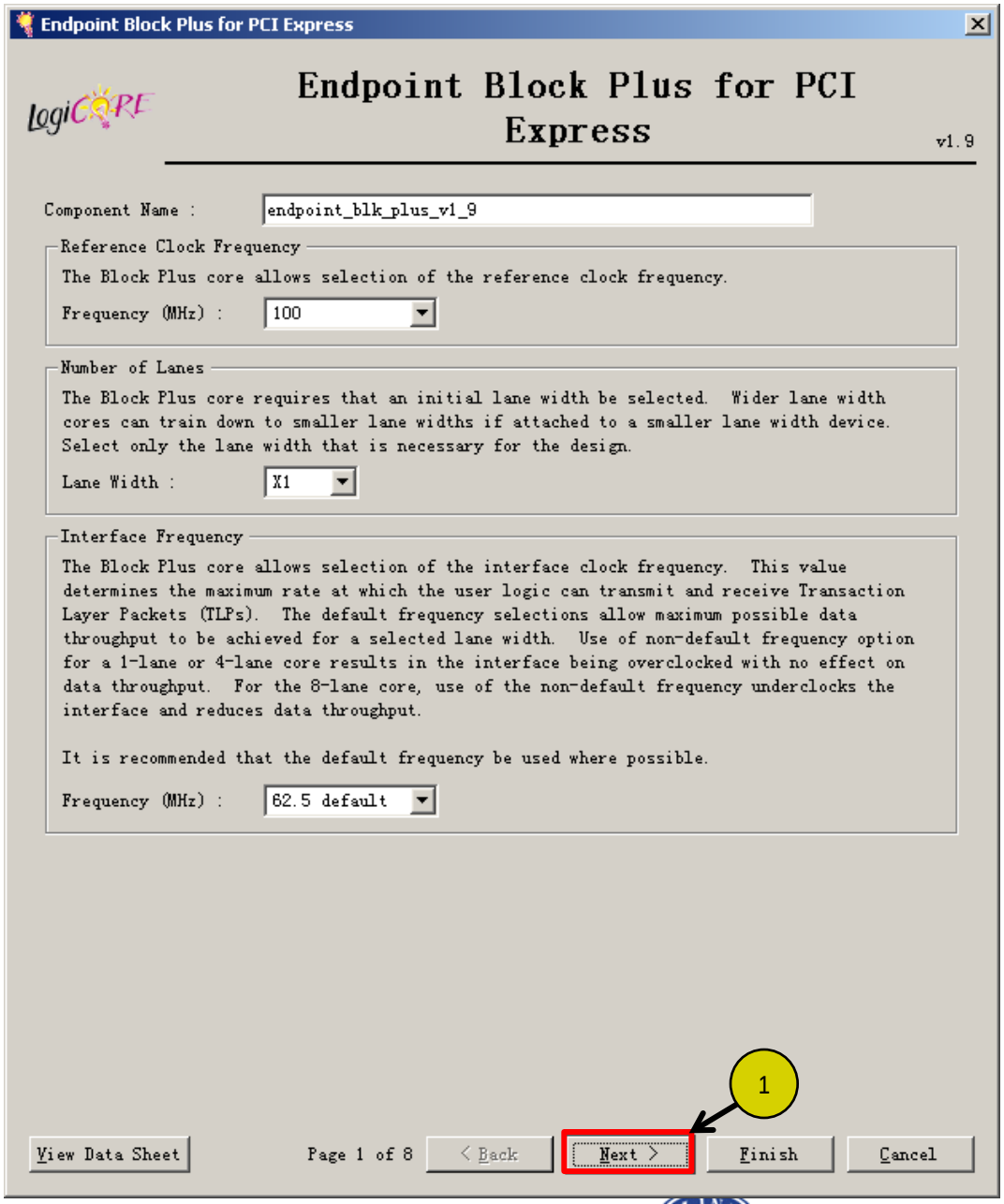
PCIe Core Generation

- Double-click on the PCI Express Endpoint Block Plus Version 1.9



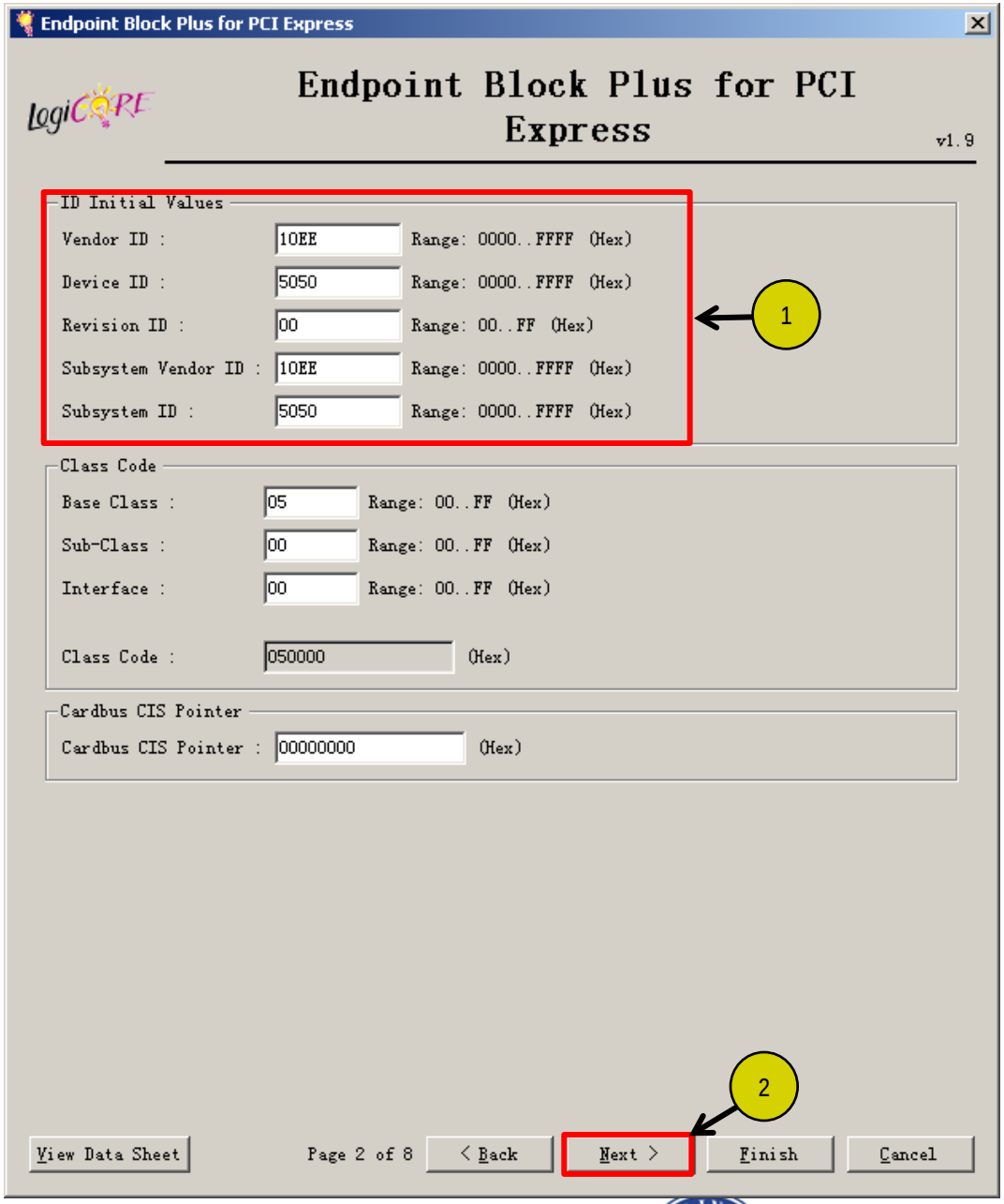
Configure PCIe Core

- Click Next(1)



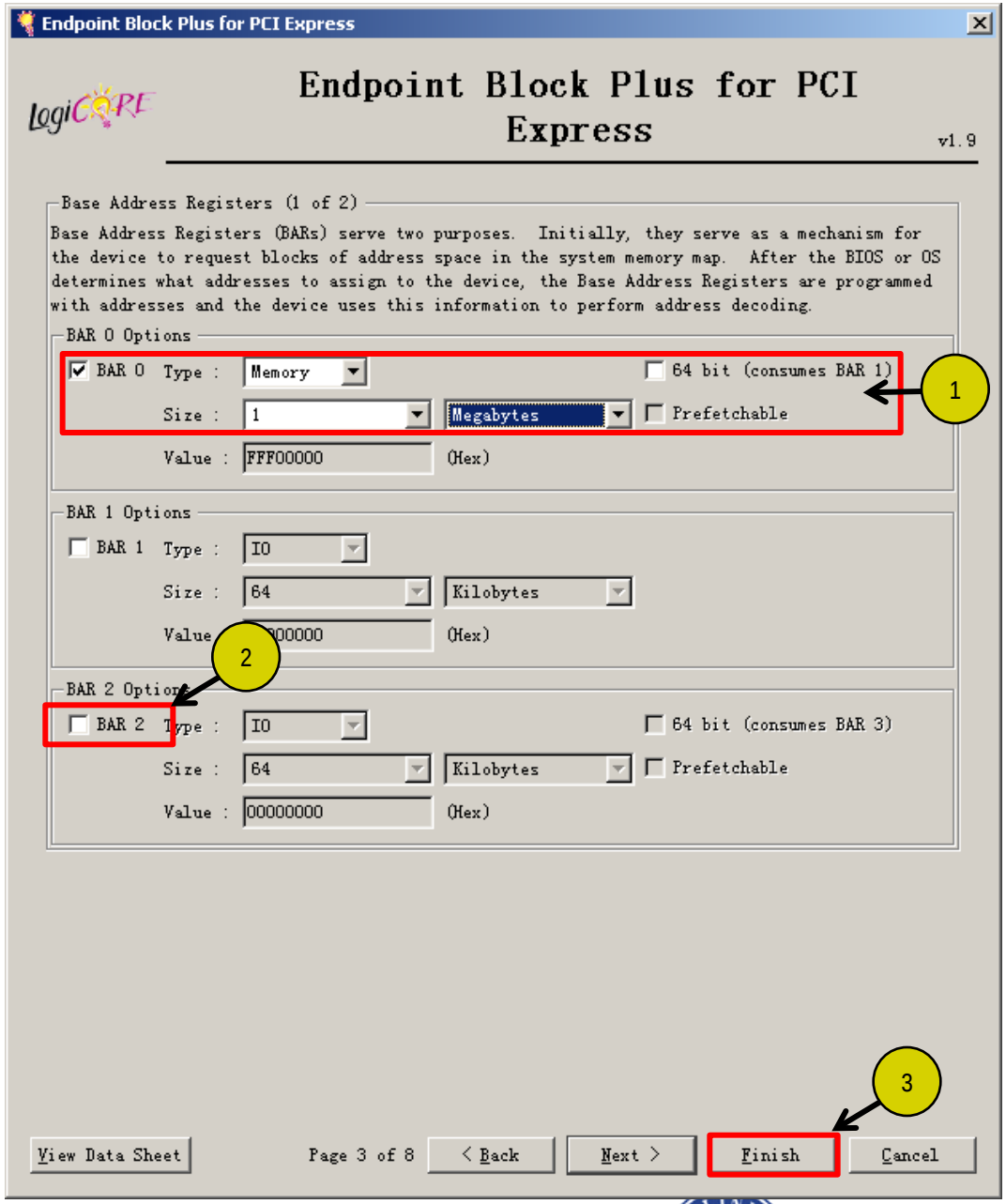
Configure PCIe Core

- Set ID Initial Values as shown (1)
- Click Next (2)



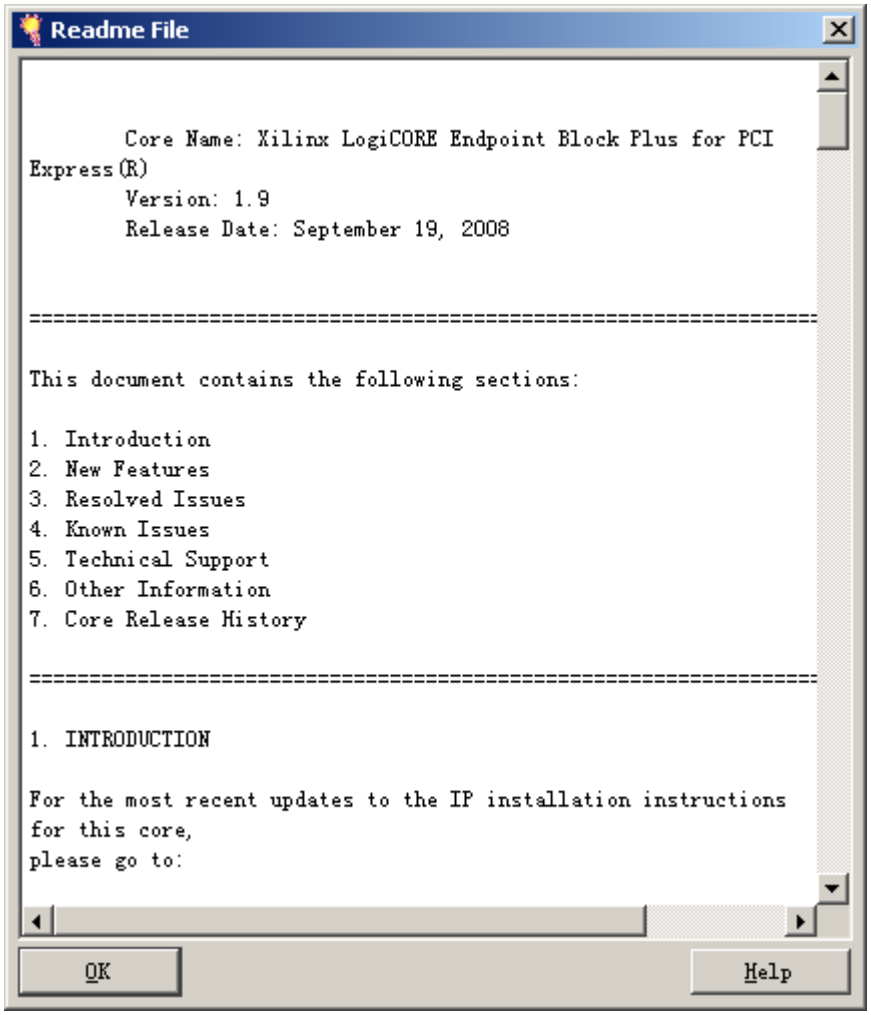
Configure PCIe Core

- Set BAR 0 to 1 Megabytes and de-select 64-bit (1)
- De-Select other BARs (2)
- Click Finish (3)



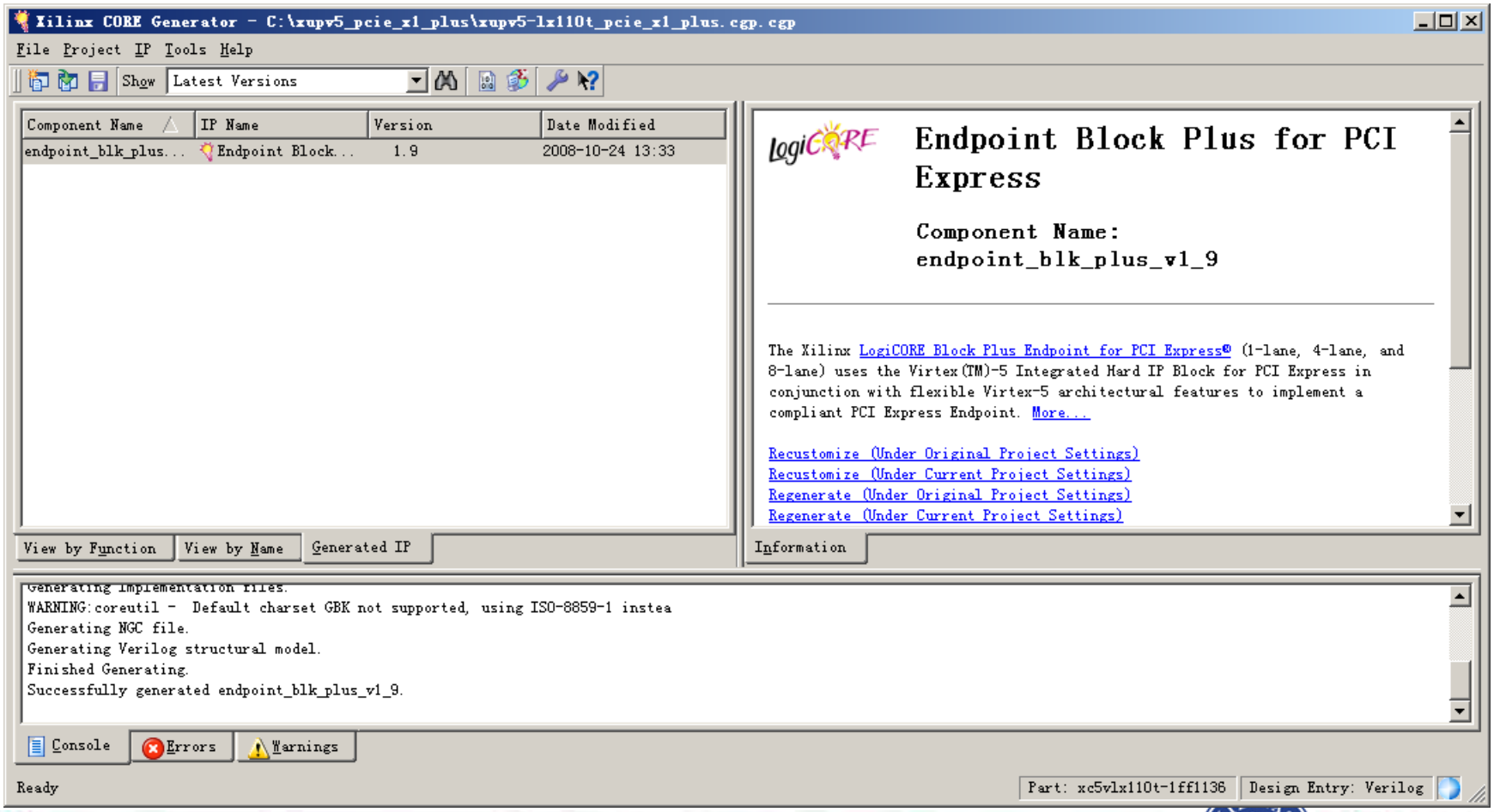
Configure PCIe Core

- After the PCIe core finishes generating, click OK on the Readme File window



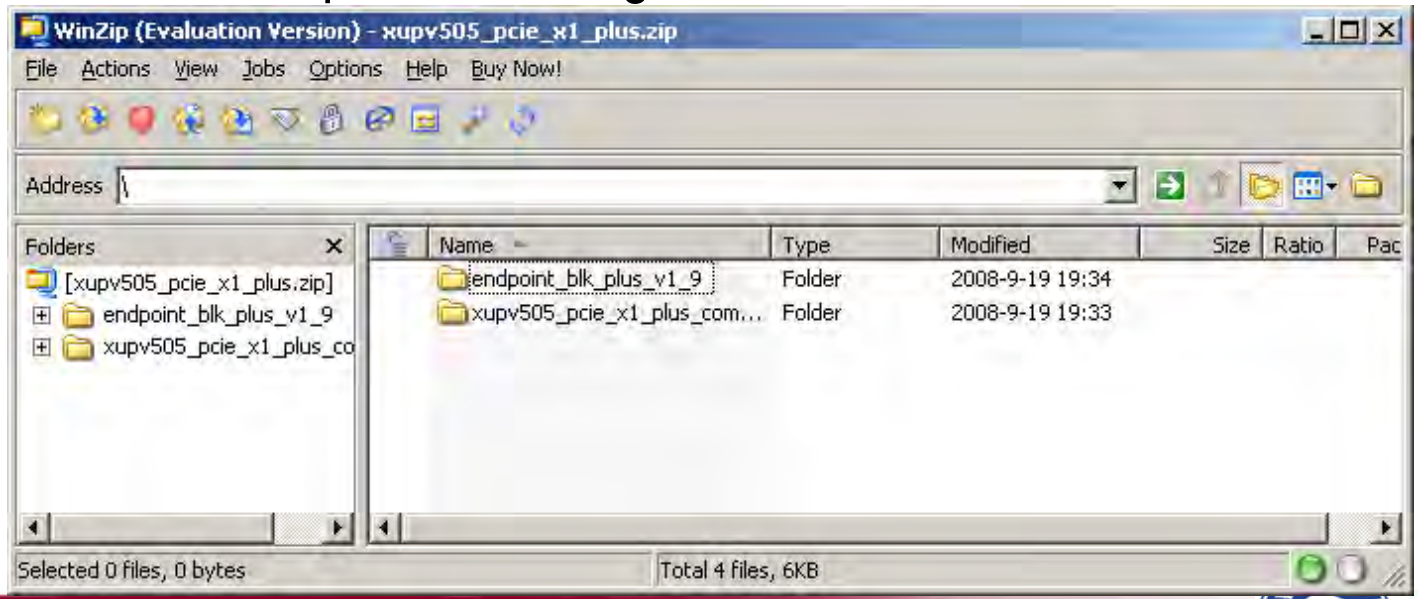
Configure PCIe Core

- The pcie_blk_plus_v1_9 IP appears under the Generated IP tab



Configure PCIe Core

- Unzip the xupv5-lx110t_pcie_x1_plus.zip file to your project directory
  - This file has been prepared for your convenience and it will add several required files as noted in the next slide
  - Includes a pre-built design with a bitstream

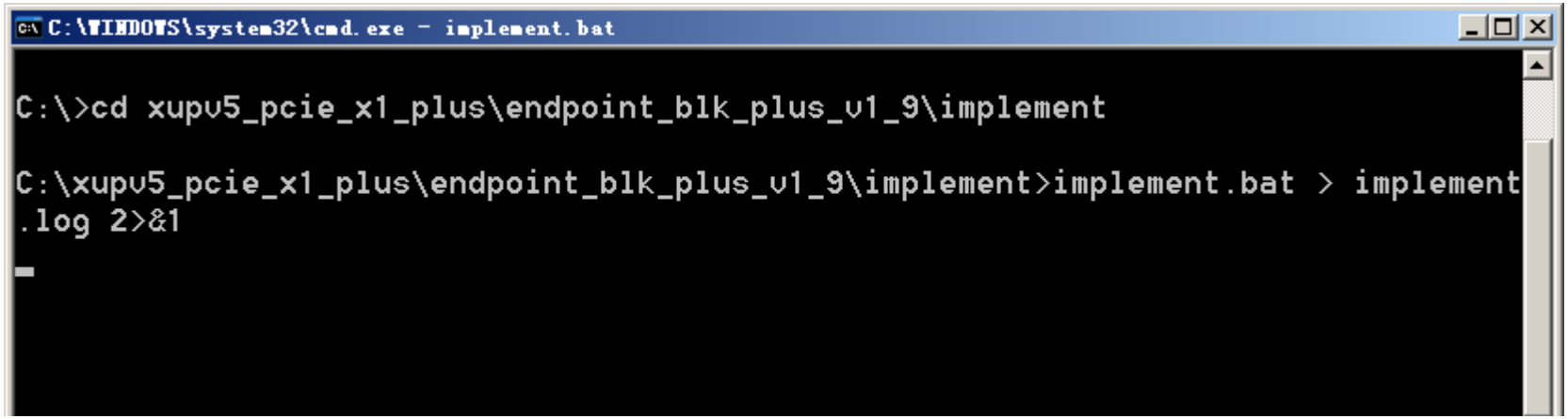


Configure PCIe Core

- The files added are:
  - These two files are required for ACE file generation
    - /implement/make_ace.bat
    - /implement/pcie_ace.cmd
  - Modification to the implementation flow (overwrites existing file)
    - /implement/implement.bat
  - UCF files specific to the XUPV5-LX110T board
    - /example_design/xupv5-lx110t_pcie_x1_plus.ucf

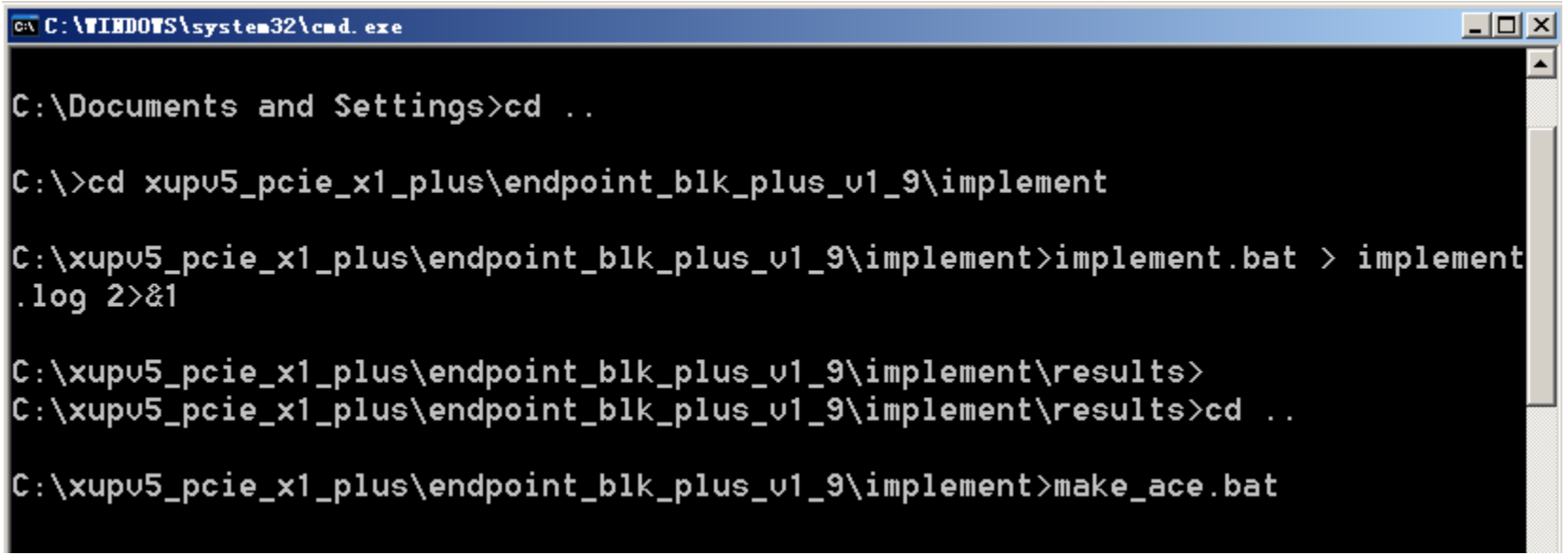
PCIe Core Compilation

- Type these commands in a windows command shell:
  - cd C:\xupv5_pcie_x1_plus\endpoint_blk_plus_v1_9\implement
  - implement.bat > implement.log 2>&1



Generate ACE File

- Type this command in a windows command shell:
  - cd ..
  - make_ace.bat

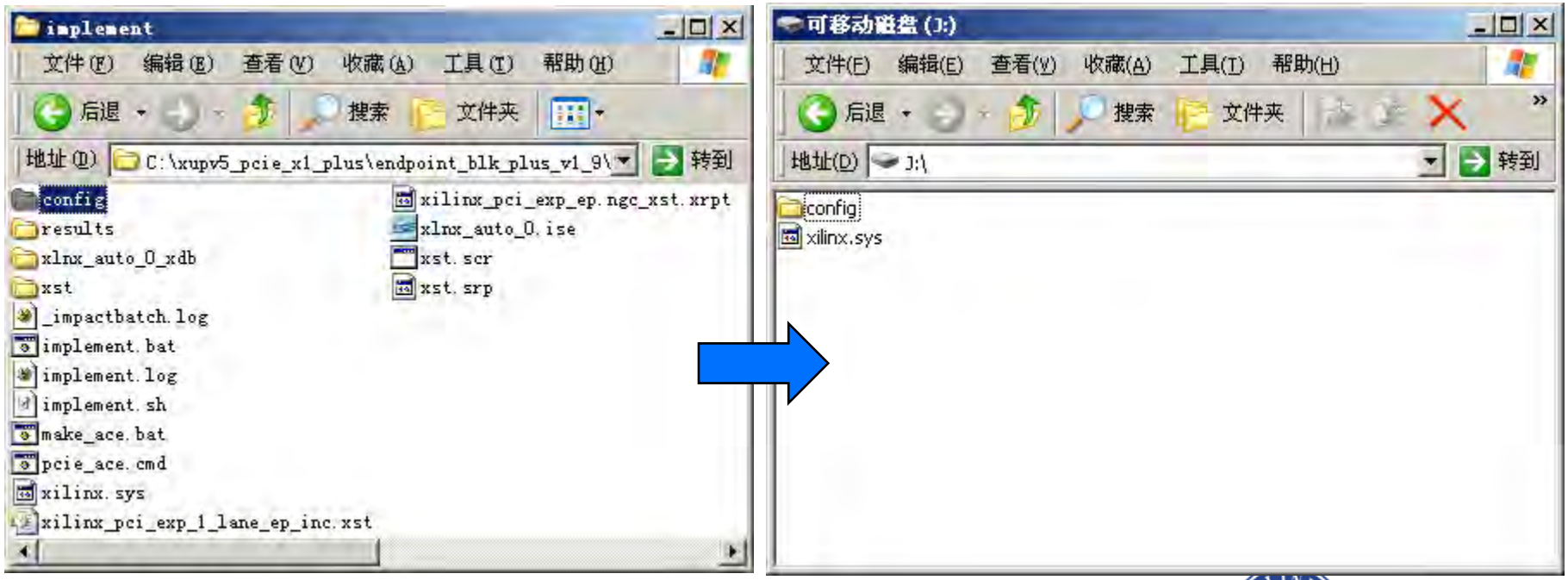


ACE File Execution

- Use a CompactFlash reader to mount the XUPV5-LX110T CompactFlash as a disk drive
- Delete any existing ace files in this <CF Drive>\config\rev6 directory
- Note: rev6 matches the DIP switch settings

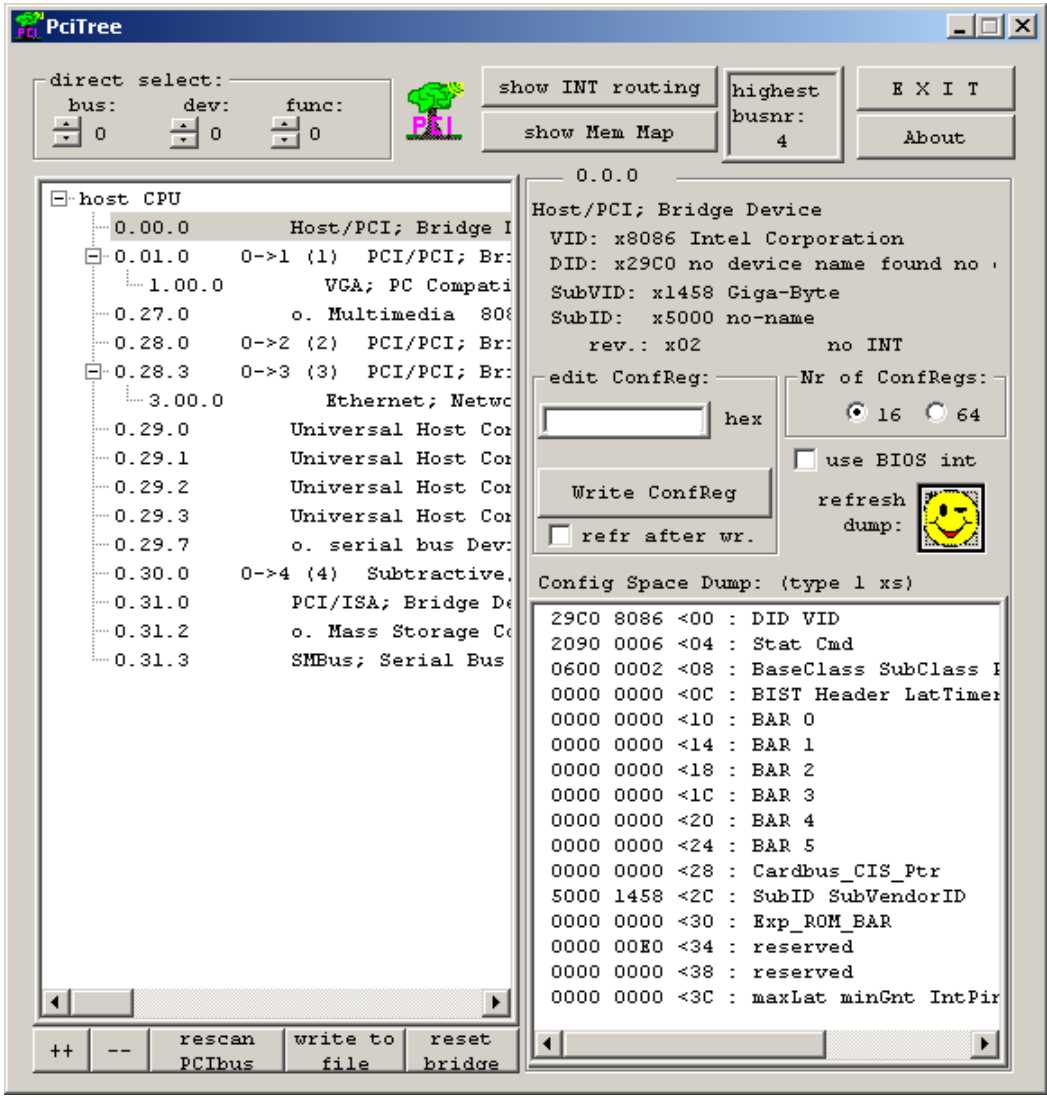
ACE File Execution

- Copy config directory, which contains generated pcie_blk_plus_top.ace, to your CompactFlash card



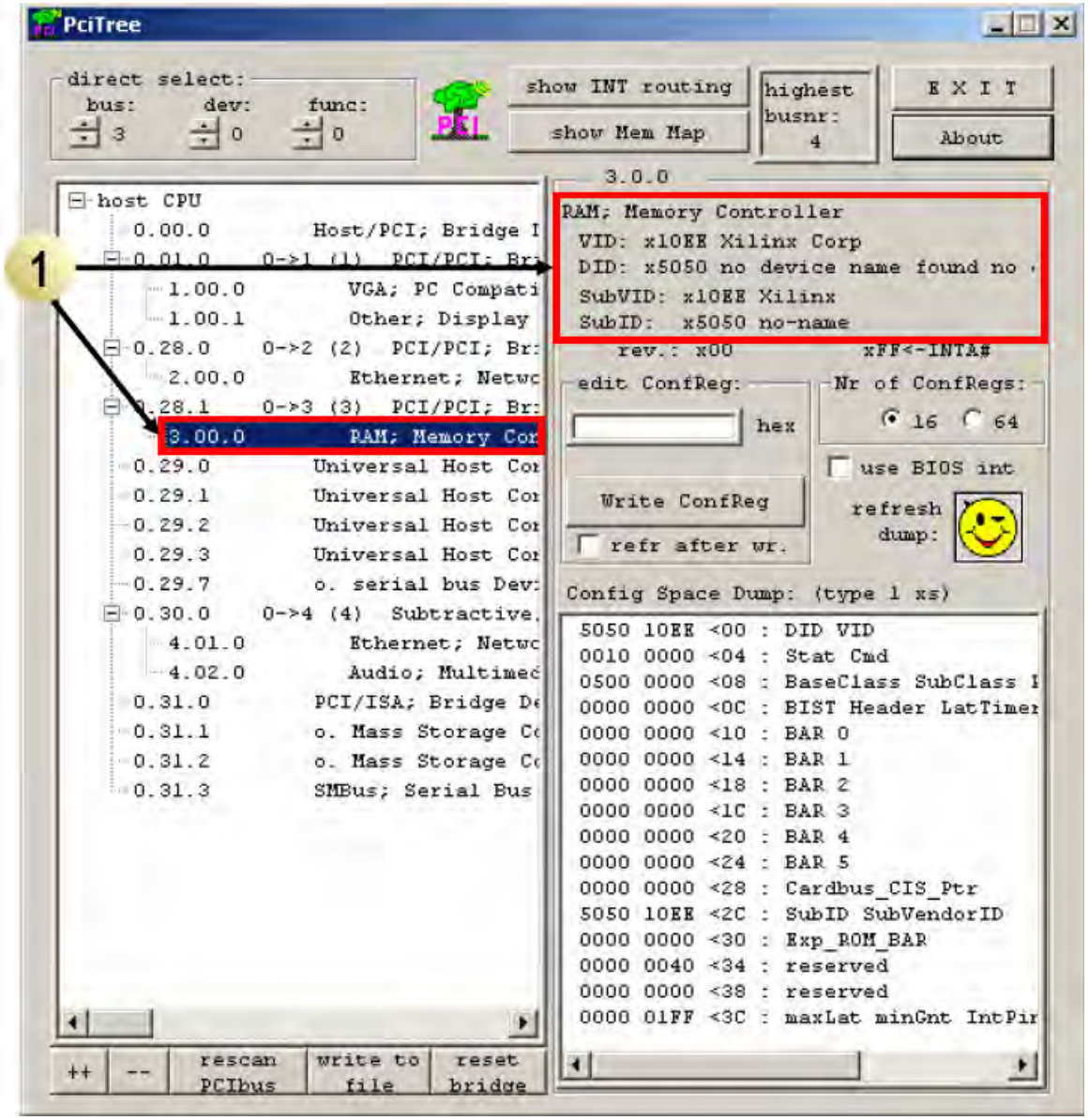
PciTree

- Eject the Compact Flash from your PC, insert it back into the XUPV5-LX110T and power-up the board
- Power on the PC
- Start PciTree



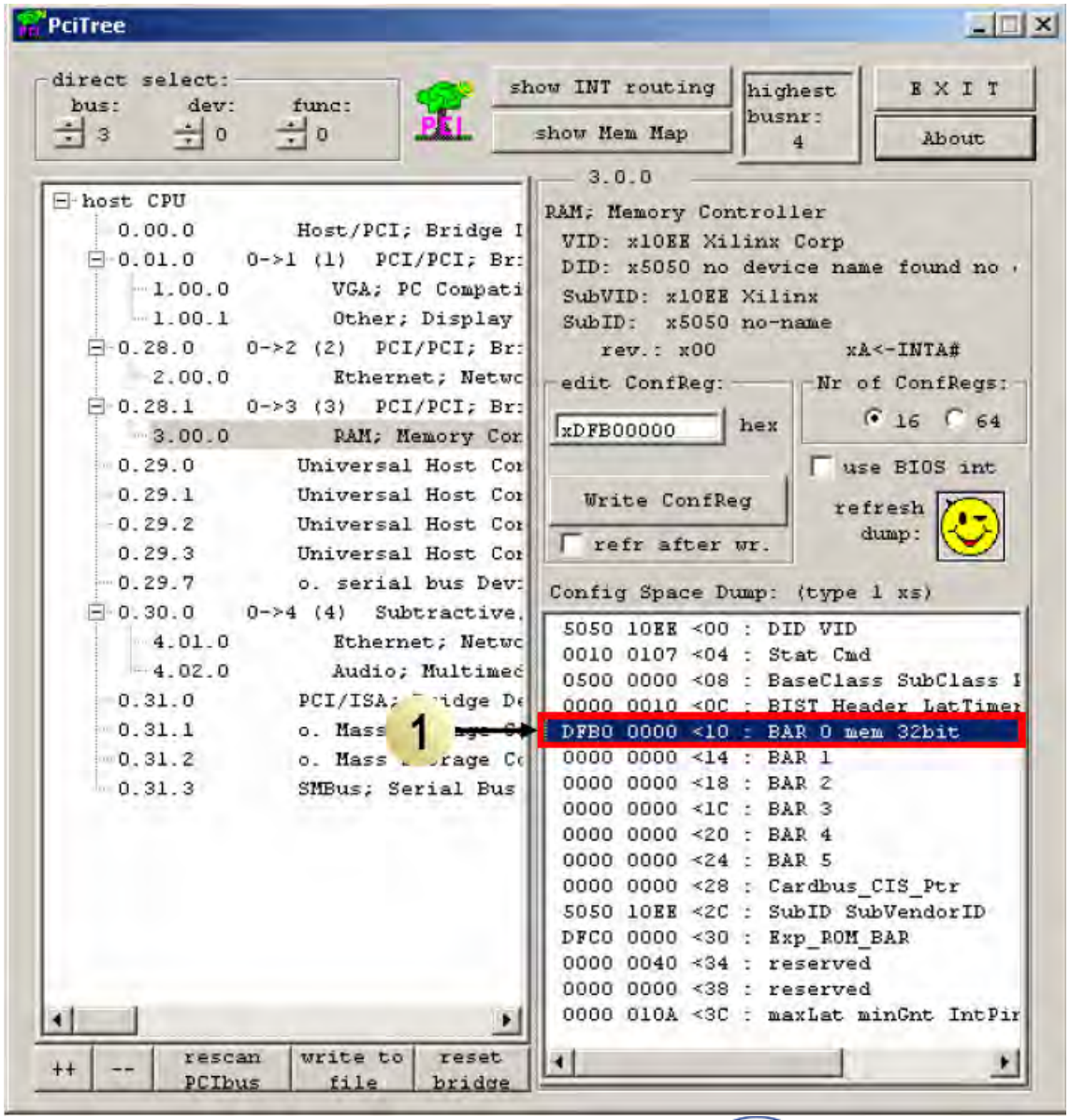
PciTree

- Locate the Xilinx Device
  - Vendor ID 10EE



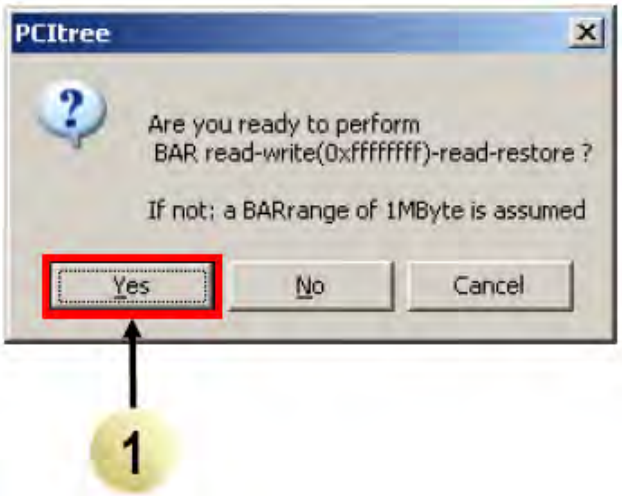
PciTree

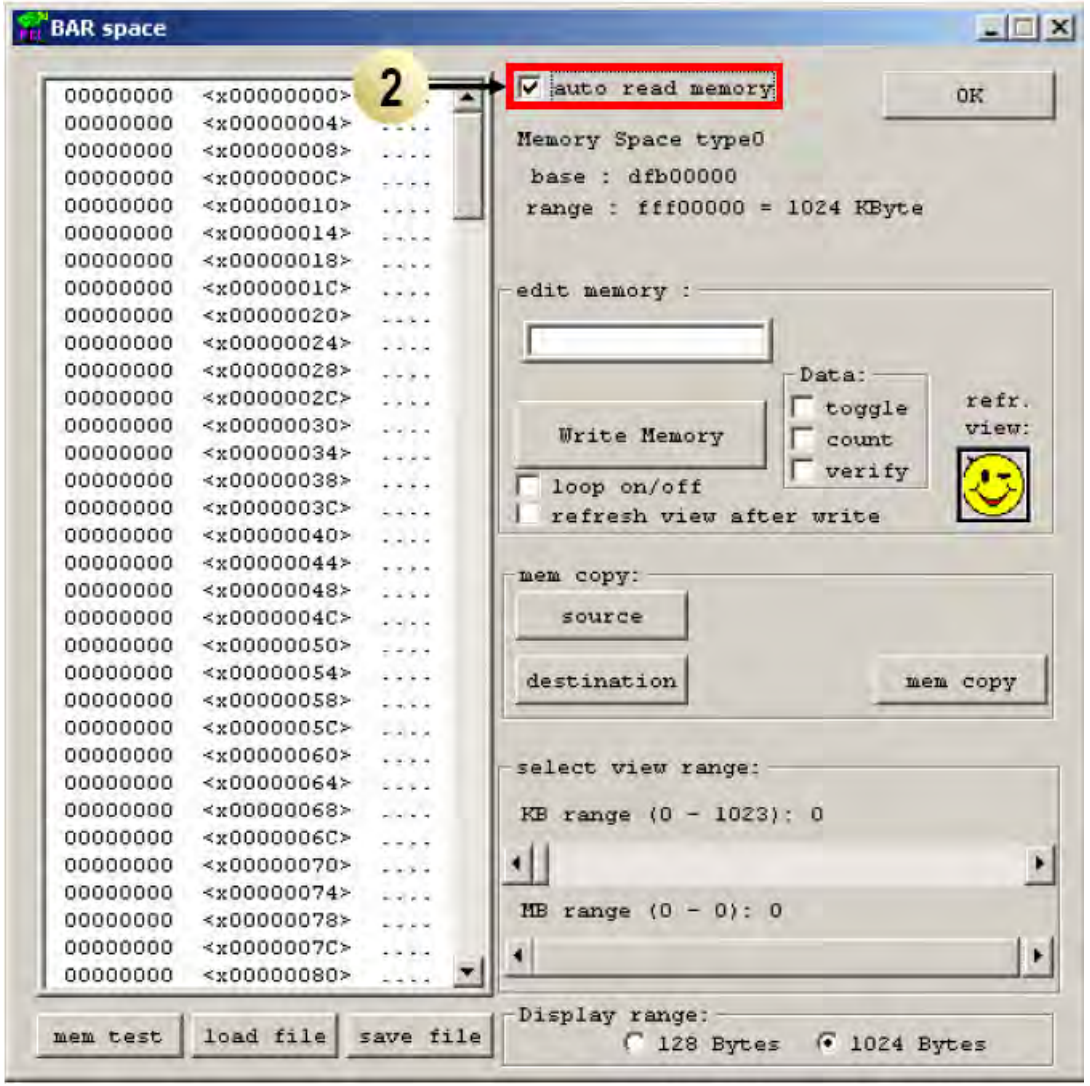
- With the Xilinx device selected, double-click on BAR 0



PciTree Bus Viewer

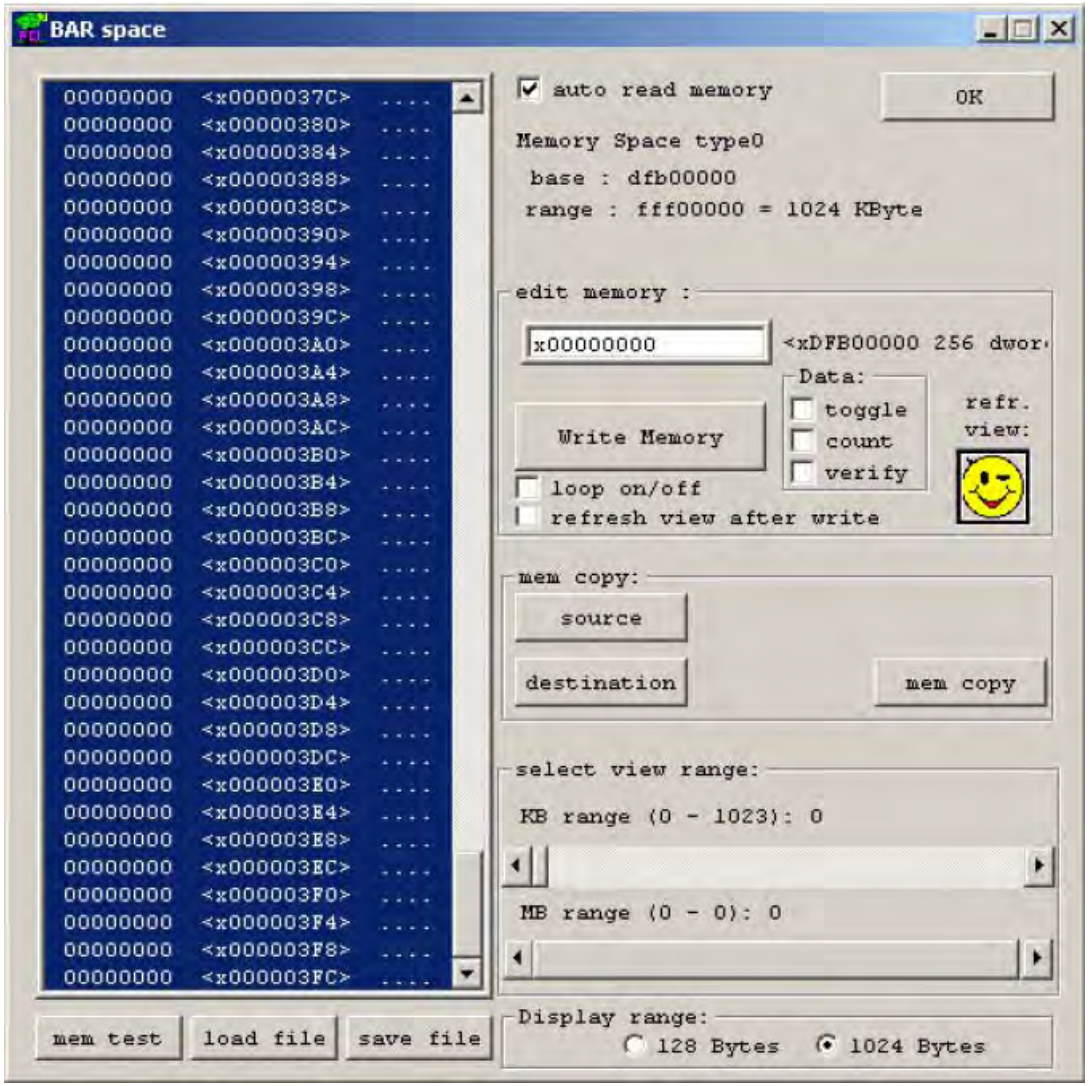
- Click Yes (1)
- Select auto read memory (2)





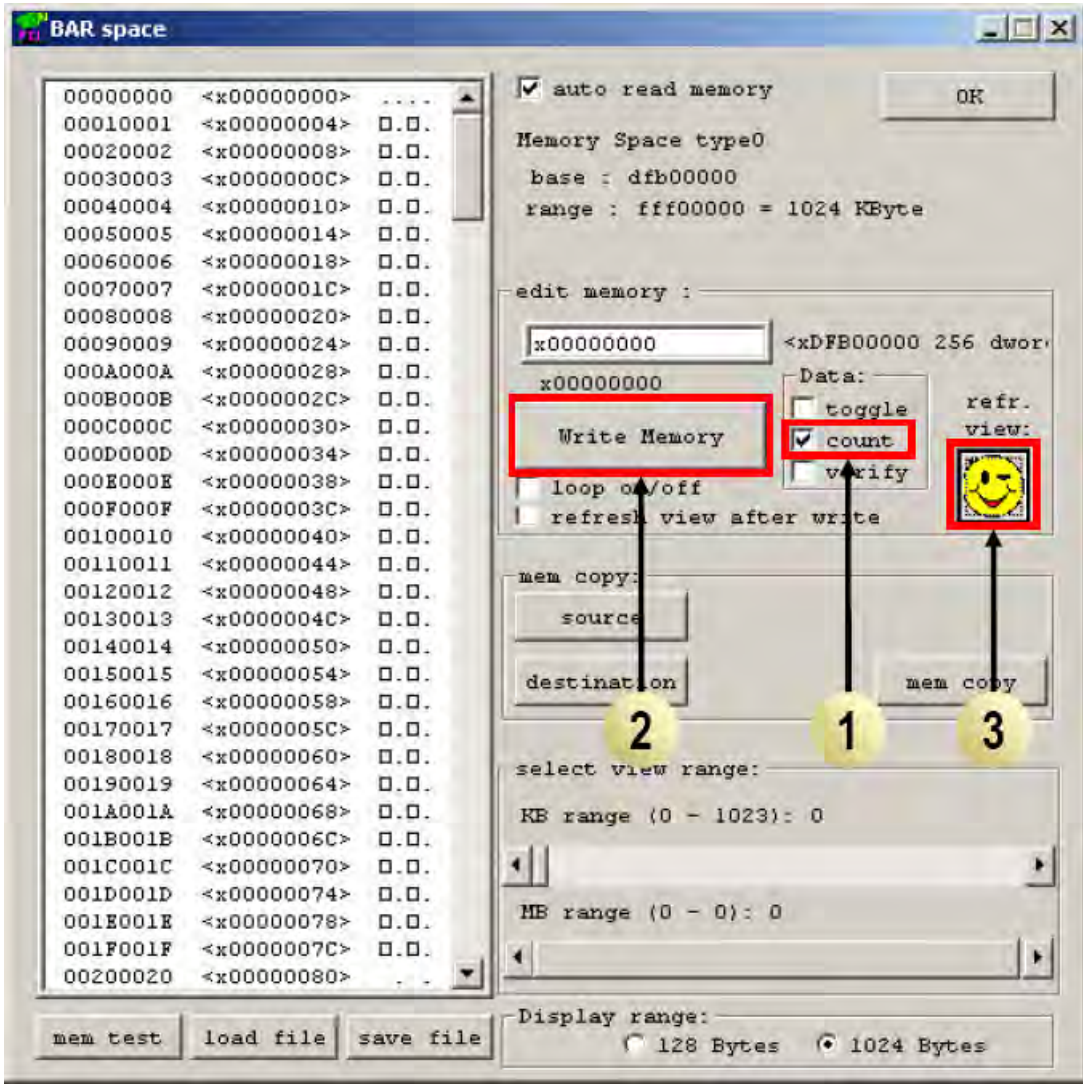
PciTree Bus Viewer

- Click on the first memory location
- Type <Shift-End> to select 1k (256 dwords)



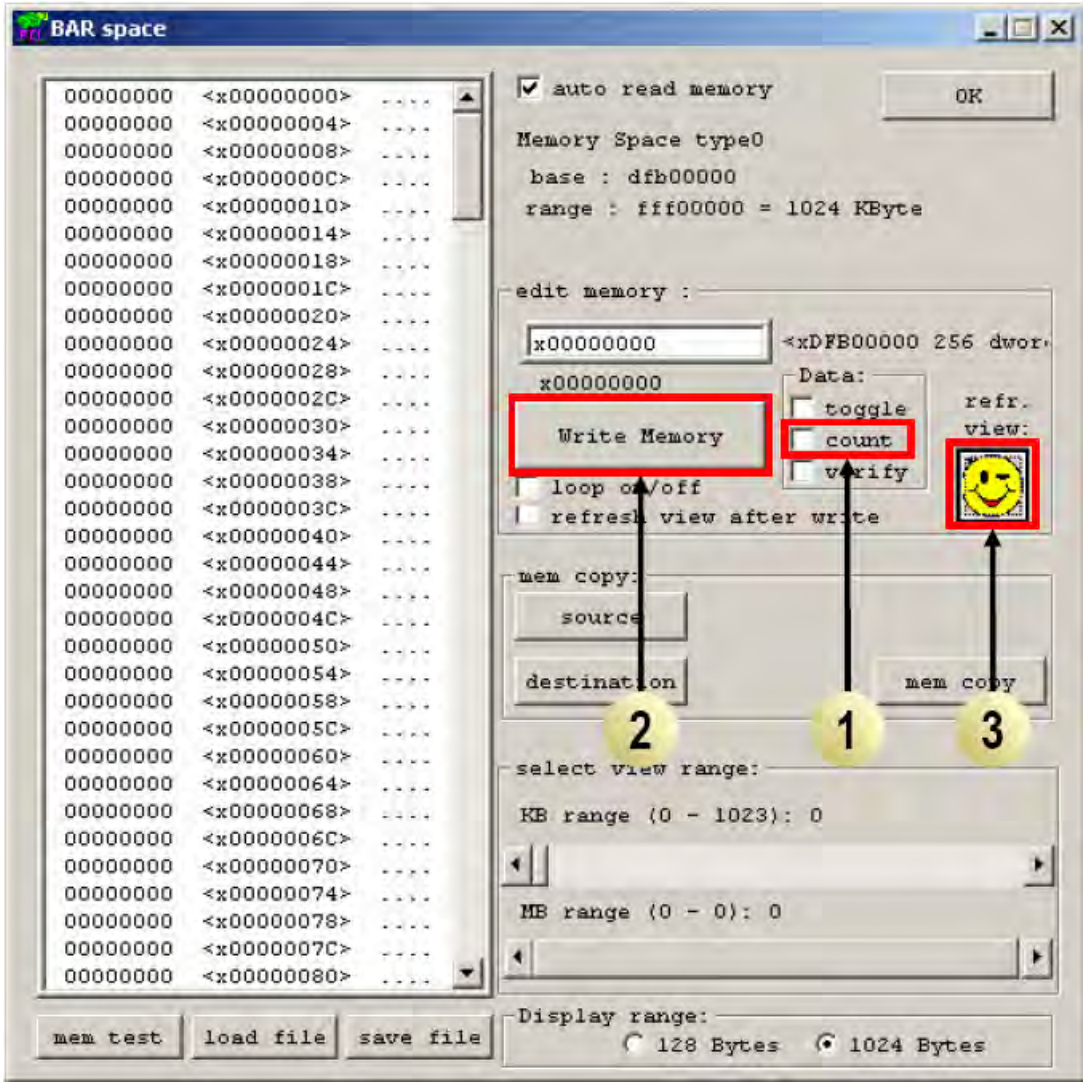
PciTree Bus Viewer

- Write Memory
  - Select count (1)
  - Click Write Memory (2)
  - Click refr view (3)
- View results
  - Counting up to FF



PciTree Bus Viewer

- Restore Memory
  - Deselect count (1)
  - Click Write Memory (2)
  - Click refr view (3)
- Memory is reset to zeros



Documentation

- Virtex-5
  - Virtex-5 FPGA User Guide
    http://www.xilinx.com/support/documentation/user_guides/ug190.pdf
  - Virtex-5 Packaging and Pinout Specification
    http://www.xilinx.com/support/documentation/user_guides/ug195.pdf
- Virtex-5 RocketIO
  - RocketIO GTP Transceiver User Guide –UG196
    http://www.xilinx.com/support/documentation/user_guides/ug196.pdf
  - RocketIO GTX Transceiver User Guide –UG198
    http://www.xilinx.com/support/documentation/user_guides/ug198.pdf

Documentation

- PCIe
  - LogiCORE Endpoint Block Plus for PCI Express Data Sheet
    http://www.xilinx.com/support/documentation/ip_documentation/pcie_blk_plus_ds551.pdf
  - LogiCORE Endpoint Block Plus for PCI Express Designs
    http://www.xilinx.com/support/documentation/ip_documentation/pcie_blk_plus_ug341.pdf
  - LogiCORE Endpoint Block Plus Getting Started Guide for PCI Express Designs
    http://www.xilinx.com/support/documentation/ip_documentation/pcie_blk_plus_gsg343.pdf
  - Virtex-5 Integrated Endpoint Block User Guide for PCI Express Designs
    http://www.xilinx.com/support/documentation/user_guides/ug197.pdf