



XUPV5-LX110T PCIe x1 Endpoint Plus Design Creation

Using ISE™ 10.1i SP3, Core generator 10.1i SP3



September, 2008

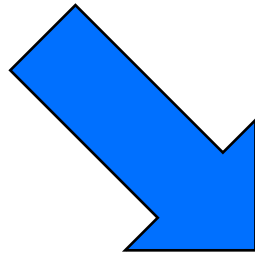
XUPV5-LX110T PCIe Overview

- Software Requirements
- Hardware Setup
- Design Creation
 - Highlighting the Virtex-5 RocketIO™ GTP/GTX Transceivers
- Testing the design



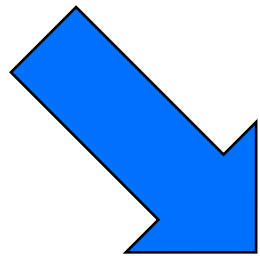
ISE Software Requirement

- Xilinx ISE 10.1i SP3 software



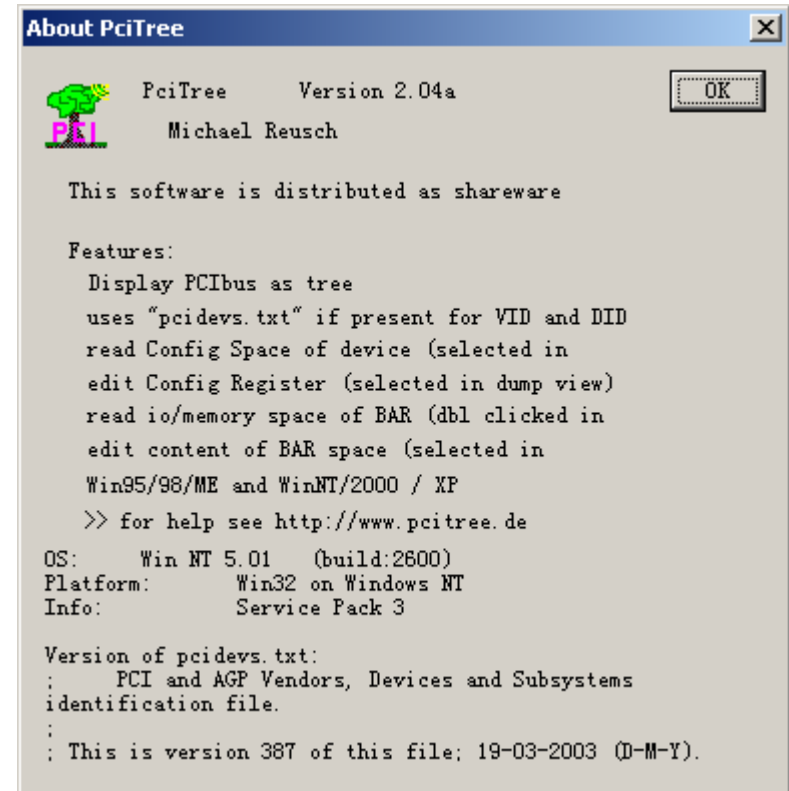
Coregen Software Requirement

- Install Xilinx Coregen 10.1i IP Update 3

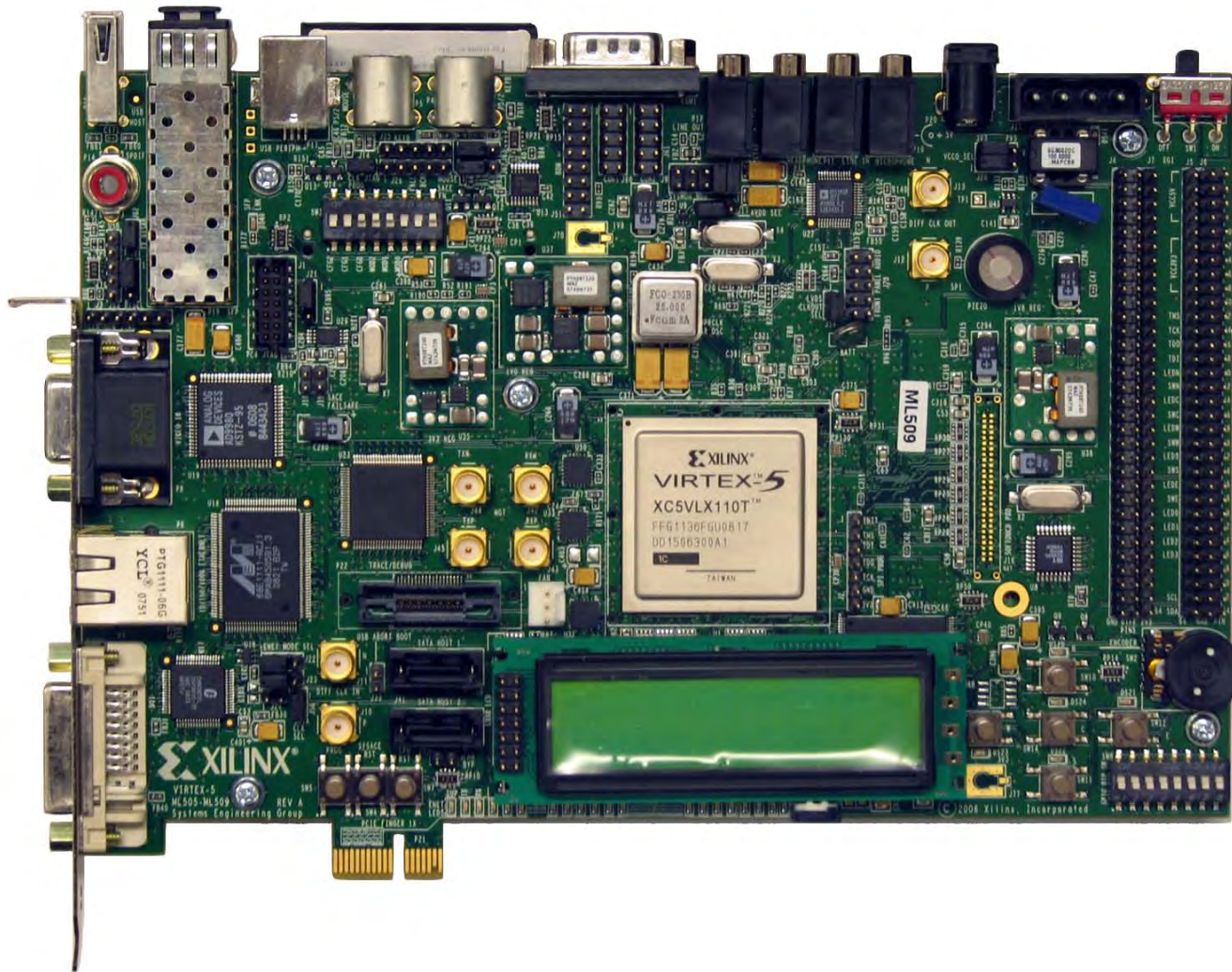


Software Requirement

- PciTree Bus Viewer
 - Free download from <http://www.pcitree.de/index.html>
 - HLP.SYS must be copied to <C:\WINDOWS\system32\drivers> directory



Xilinx XUPV5-LX110T Board

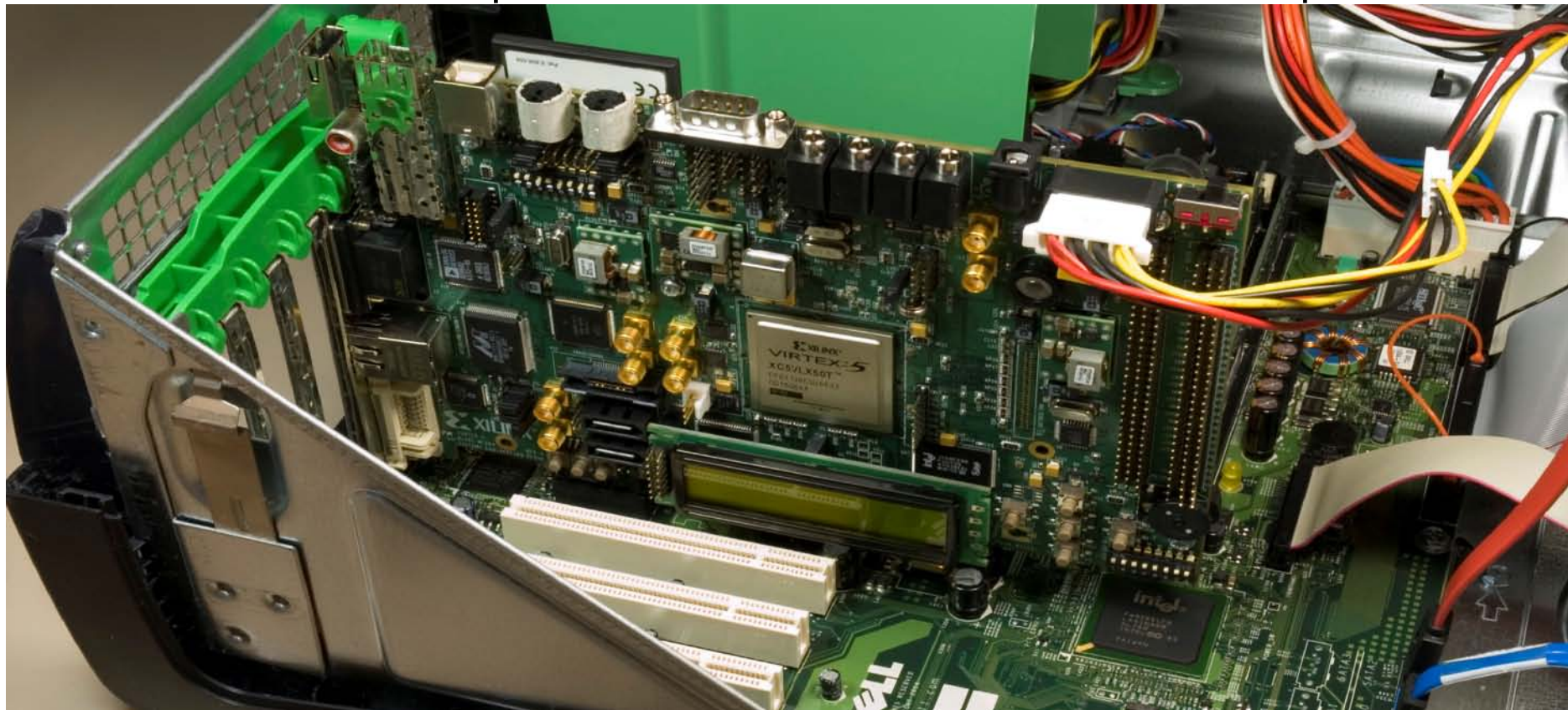


Note: The XUPV5-LX110T uses an XC5VLX110T FPGA.



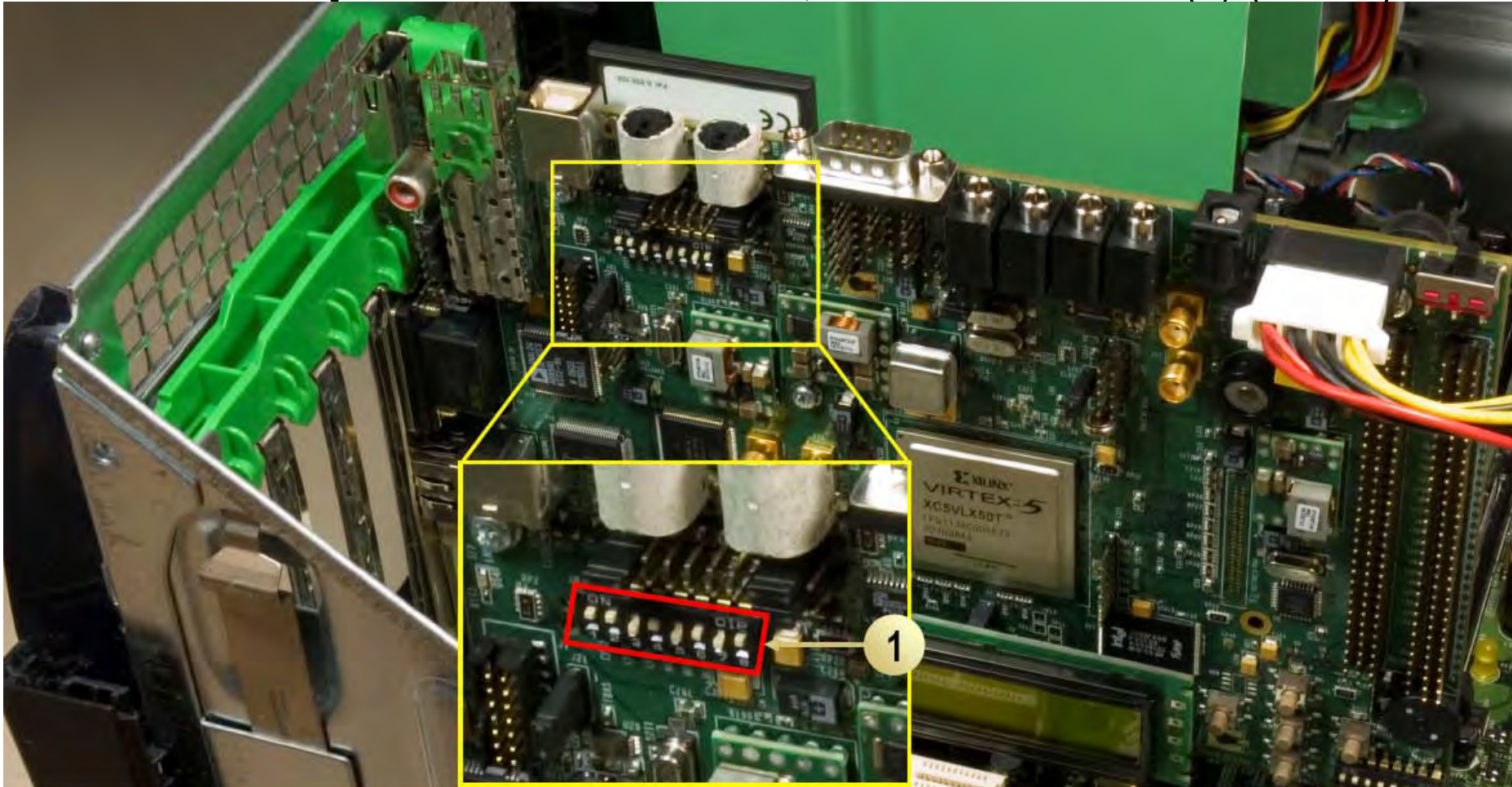
Setting Up the Hardware

- Insert the XUPV5-LX110T Board into a PCIe x1 slot
 - Connect PC power or use XUPV5-LX110T Power Adapter



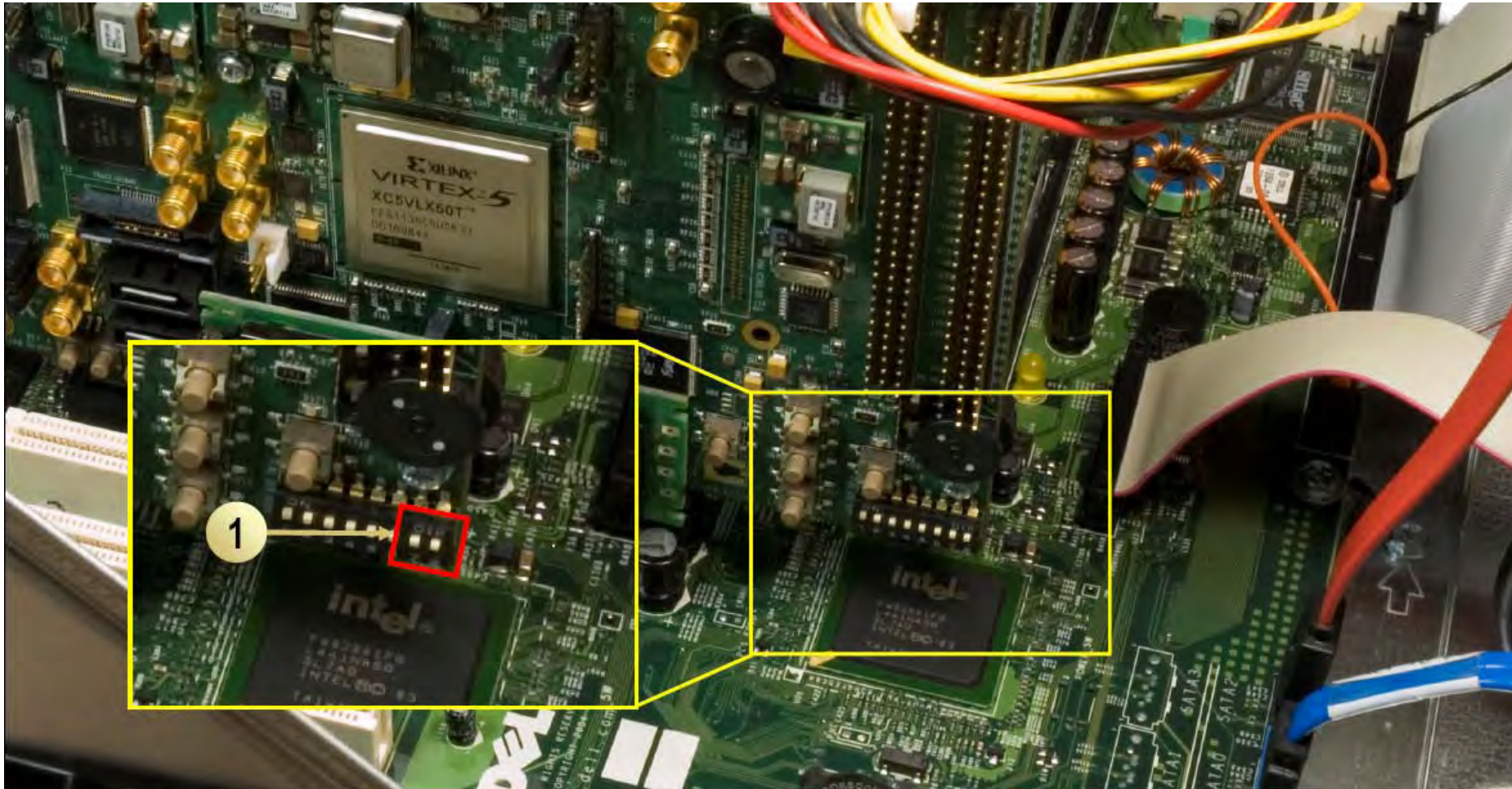
Setting Up the Hardware

- Set the System ACE DIP switches, SW3 to 11010101 (1) (1 = on)



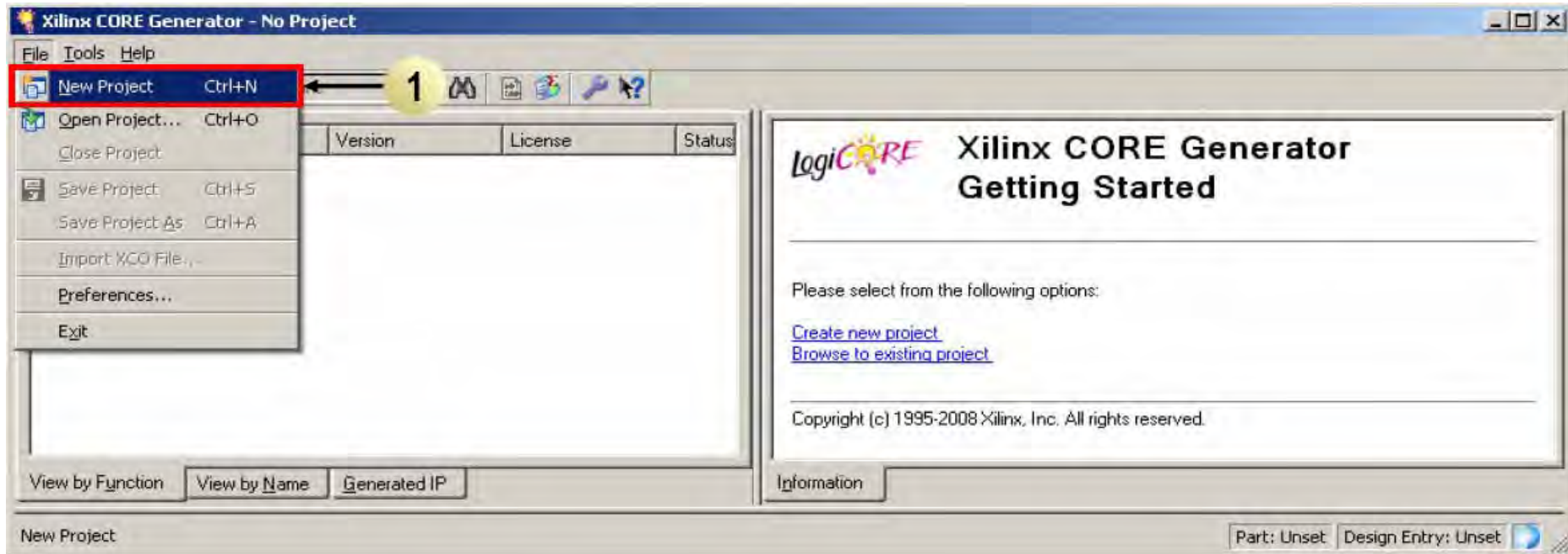
Setting Up the Hardware

- Set DIP Switch SW8, bit 7 & 8 to up as per [AR24826](#)



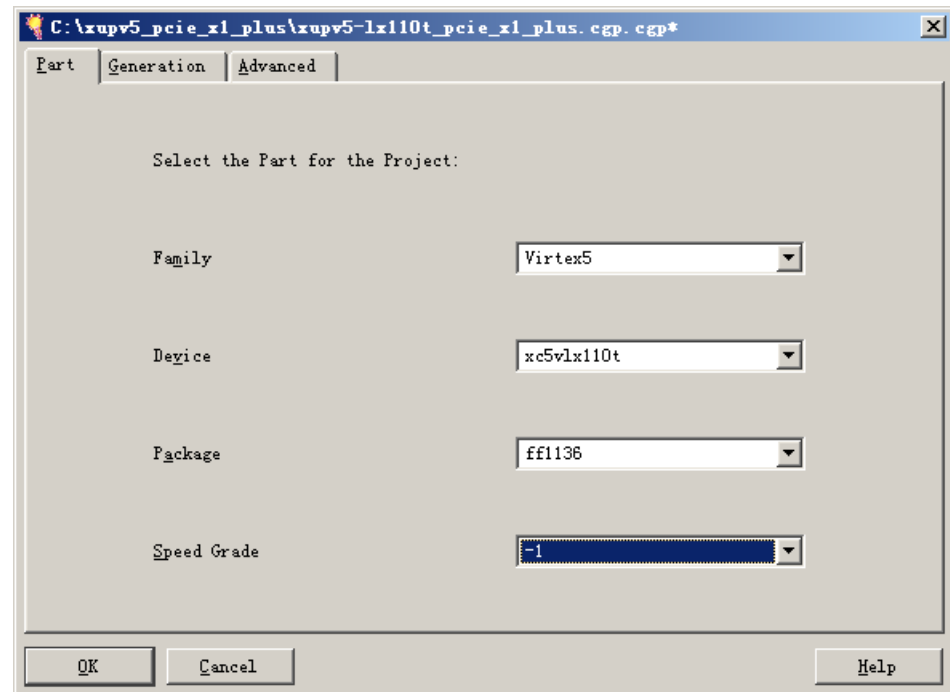
CORE Generator

- Open the CORE Generator
 - Start → All Programs → Xilinx ISE Design Suite 10.1i → ISE → Accessories → CORE Generator
- Create a new project; select File → New Project (1)



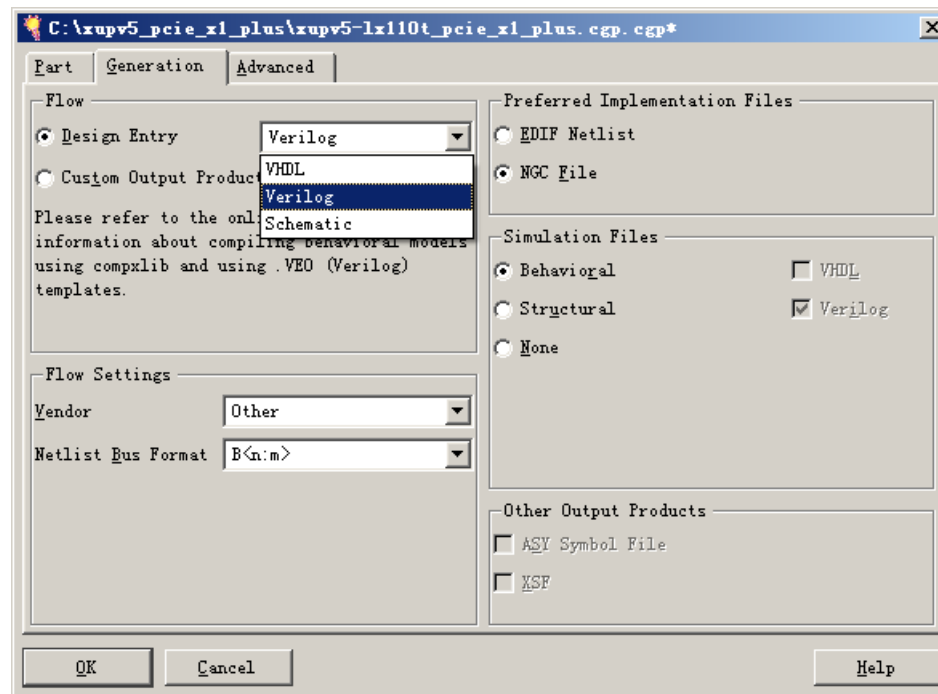
PCIe Core Generation

- Create a project directory: xupv5_pcie_x1_plus
- Name the project: xupv5-lx110t_pcie_x1_plus.cgp
- Set the Part:
 - Family: Virtex5
 - Device: xc5vlx110t
 - Package: ff1136
 - Speed Grade: -1



PCIe Core Generation

- Set the Design Entry to Verilog
- Click OK



PCIe Core Generation

- Double-click on the PCI Express Endpoint Block Plus Version 1.9

The screenshot shows the Xilinx CORE Generator interface. The left pane displays a tree view of functions, with 'PCI Express' expanded to show 'Endpoint Bloc... 1.9', 'Endpoint for ... 3.6', and 'Endpoint PIPE... 1.7'. A context menu is open over 'Endpoint Bloc... 1.9', with 'Customize' selected. The right pane displays the 'Endpoint Block Plus for PCI Express' information page, including a description, links for 'Customize', 'View Data Sheet', 'View License Status', 'View Product Webpage', 'View Version Information', and 'View Answer Records', and a section for 'Families supported:'. The bottom console shows a welcome message and the project file path.

Xilinx CORE Generator - C:\xupv5_pcie_xl_plus\xupv5-lx110t_pcie_xl_plus.cgp.cgp

File Project IP Tools Help

Show Latest Versions

Function	Version	License	Stat
Debug & Verification			
Digital Signal Proc...			
FPGA Features and D...			
Math Functions			
Memories & Storage ...			
Standard Bus Interfaces			
LVDS			
PCI			
PCI Express			
Endpoint Bloc... 1.9			
Endpoint for ... 3.6			
Endpoint PIPE... 1.7			
RapidIO			
Storage, NAS and SAN			
Video & Image Proce...			

View by Function View by Name

Endpoint Block Plus for PCI Express

The Xilinx [LogiCORE Block Plus Endpoint for PCI Express®](#) (1-lane, 4-lane, and 8-lane) uses the Virtex(TM)-5 Integrated Hard IP Block for PCI Express in conjunction with flexible Virtex-5 architectural features to implement a compliant PCI Express Endpoint. [More...](#)

[Customize](#)
[View Data Sheet](#)
[View License Status](#)
[View Product Webpage](#)
[View Version Information](#)
[View Answer Records](#)

Families supported:

Information

Welcome to Xilinx CORE Generator.
Wrote project file C:\xupv5_pcie_xl_plus\xupv5-lx110t_pcie_xl_plus.cgp.cgp.

Console Errors Warnings

Ready

Part: xc5vlx110t-1ff1136 Design Entry: Verilog



Configure PCIe Core

- Click Next(1)

Endpoint Block Plus for PCI Express v1.9

Component Name : endpoint_blk_plus_v1_9

Reference Clock Frequency
The Block Plus core allows selection of the reference clock frequency.
Frequency (MHz) : 100

Number of Lanes
The Block Plus core requires that an initial lane width be selected. Wider lane width cores can train down to smaller lane widths if attached to a smaller lane width device. Select only the lane width that is necessary for the design.
Lane Width : X1

Interface Frequency
The Block Plus core allows selection of the interface clock frequency. This value determines the maximum rate at which the user logic can transmit and receive Transaction Layer Packets (TLPs). The default frequency selections allow maximum possible data throughput to be achieved for a selected lane width. Use of non-default frequency option for a 1-lane or 4-lane core results in the interface being overclocked with no effect on data throughput. For the 8-lane core, use of the non-default frequency underclocks the interface and reduces data throughput.
It is recommended that the default frequency be used where possible.
Frequency (MHz) : 62.5 default

View Data Sheet Page 1 of 8 < Back Next > Finish Cancel



Configure PCIe Core

- Set ID Initial Values as shown (1)
- Click Next (2)

Endpoint Block Plus for PCI Express

logiCORE

Endpoint Block Plus for PCI Express v1.9

ID Initial Values

Vendor ID :	<input type="text" value="10EE"/>	Range: 0000..FFFF (Hex)
Device ID :	<input type="text" value="5050"/>	Range: 0000..FFFF (Hex)
Revision ID :	<input type="text" value="00"/>	Range: 00..FF (Hex)
Subsystem Vendor ID :	<input type="text" value="10EE"/>	Range: 0000..FFFF (Hex)
Subsystem ID :	<input type="text" value="5050"/>	Range: 0000..FFFF (Hex)

Class Code

Base Class :	<input type="text" value="05"/>	Range: 00..FF (Hex)
Sub-Class :	<input type="text" value="00"/>	Range: 00..FF (Hex)
Interface :	<input type="text" value="00"/>	Range: 00..FF (Hex)

Class Code : (Hex)

Cardbus CIS Pointer

Cardbus CIS Pointer : (Hex)

View Data Sheet Page 2 of 8 < Back **Next >** Finish Cancel



Configure PCIe Core

- Set BAR 0 to 1 Megabytes and de-select 64-bit (1)
- De-Select other BARs (2)
- Click Finish (3)

Endpoint Block Plus for PCI Express

LogiCORE

Endpoint Block Plus for PCI Express Express

v1.9

Base Address Registers (1 of 2)

Base Address Registers (BARs) serve two purposes. Initially, they serve as a mechanism for the device to request blocks of address space in the system memory map. After the BIOS or OS determines what addresses to assign to the device, the Base Address Registers are programmed with addresses and the device uses this information to perform address decoding.

BAR 0 Options

BAR 0 Type : Memory 64 bit (consumes BAR 1)

Size : 1 Megabytes Prefetchable

Value : FFF00000 (Hex)

BAR 1 Options

BAR 1 Type : IO

Size : 64 Kilobytes

Value : 00000000 (Hex)

BAR 2 Options

BAR 2 Type : IO 64 bit (consumes BAR 3)

Size : 64 Kilobytes Prefetchable

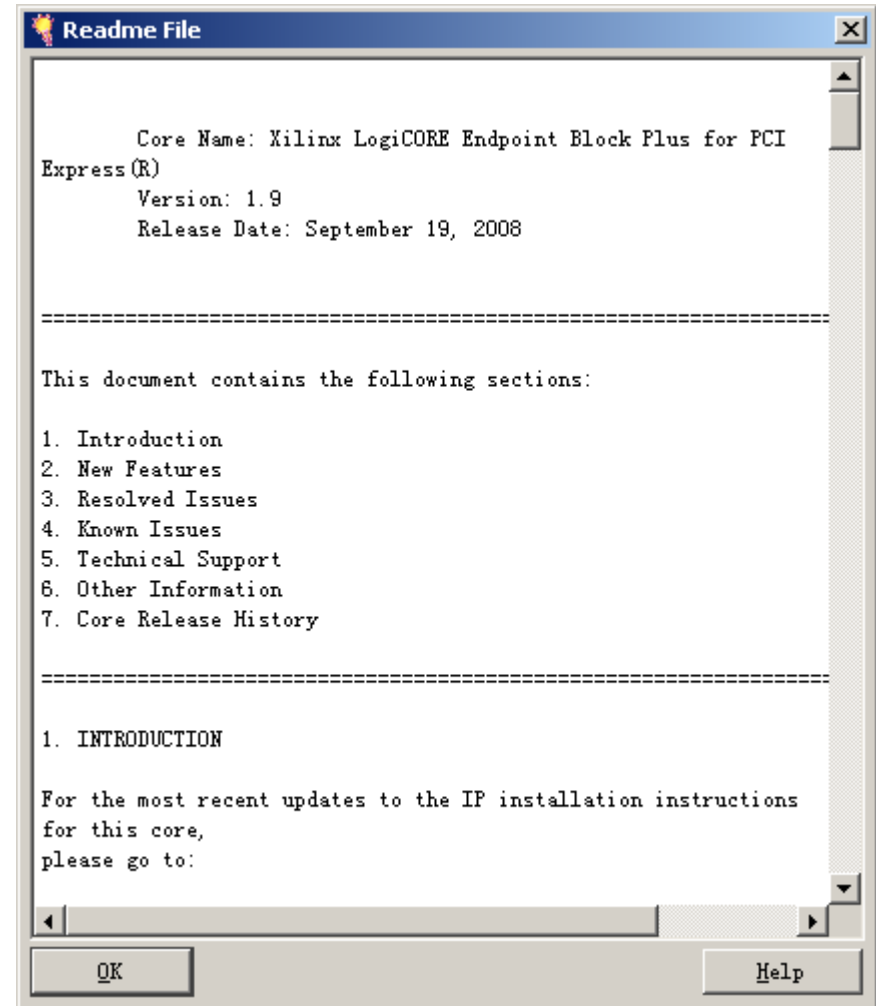
Value : 00000000 (Hex)

View Data Sheet Page 3 of 8 < Back Next > Finish Cancel



Configure PCIe Core

- After the PCIe core finishes generating, click OK on the Readme File window



Configure PCIe Core

- The `pcie_blk_plus_v1_9` IP appears under the Generated IP tab

The screenshot shows the Xilinx CORE Generator interface. The title bar reads "Xilinx CORE Generator - C:\xupv5_pcie_xl_plus\xupv5-1x110t_pcie_xl_plus.cgp.cgp". The menu bar includes "File", "Project", "IP", "Tools", and "Help". The toolbar shows "Show" and "Latest Versions".

The main window is divided into two panes. The left pane displays a table of components:

Component Name	IP Name	Version	Date Modified
endpoint_blk_plus...	Endpoint Block...	1.9	2008-10-24 13:33

The right pane, titled "Endpoint Block Plus for PCI Express", shows the component name "endpoint_blk_plus_v1_9" and a description: "The Xilinx LogiCORE Block Plus Endpoint for PCI Express® (1-lane, 4-lane, and 8-lane) uses the Virtex(TM)-5 Integrated Hard IP Block for PCI Express in conjunction with flexible Virtex-5 architectural features to implement a compliant PCI Express Endpoint. [More...](#)". Below the description are four links: "Recustomize (Under Original Project Settings)", "Recustomize (Under Current Project Settings)", "Regenerate (Under Original Project Settings)", and "Regenerate (Under Current Project Settings)".

At the bottom of the window, the "Console" pane shows the following output:

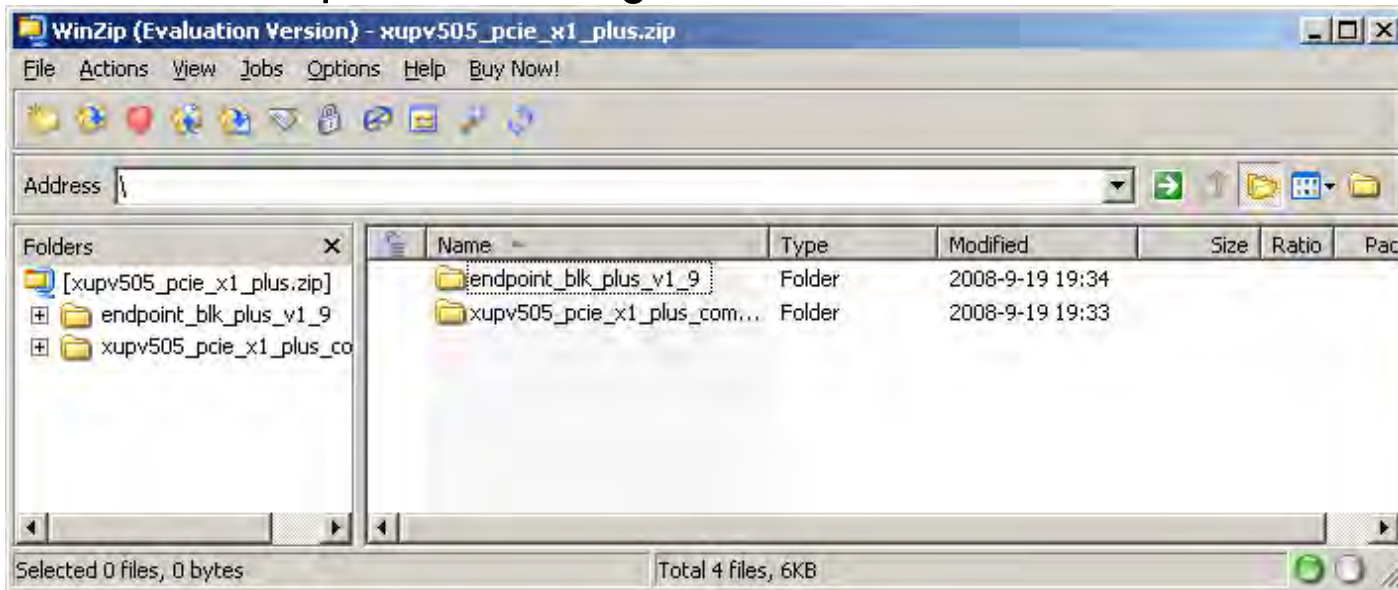
```
Generating implementation files.  
WARNING:coreutil - Default charset GBK not supported, using ISO-8859-1 instead  
Generating NGC file.  
Generating Verilog structural model.  
Finished Generating.  
Successfully generated endpoint_blk_plus_v1_9.
```

The status bar at the bottom indicates "Ready" and "Part: xc5vlx110t-1ff1136 Design Entry: Verilog".



Configure PCIe Core

- Unzip the xupv5-lx110t_pcie_x1_plus.zip file to your project directory
 - This file has been prepared for your convenience and it will add several required files as noted in the next slide
 - Includes a pre-built design with a bitstream



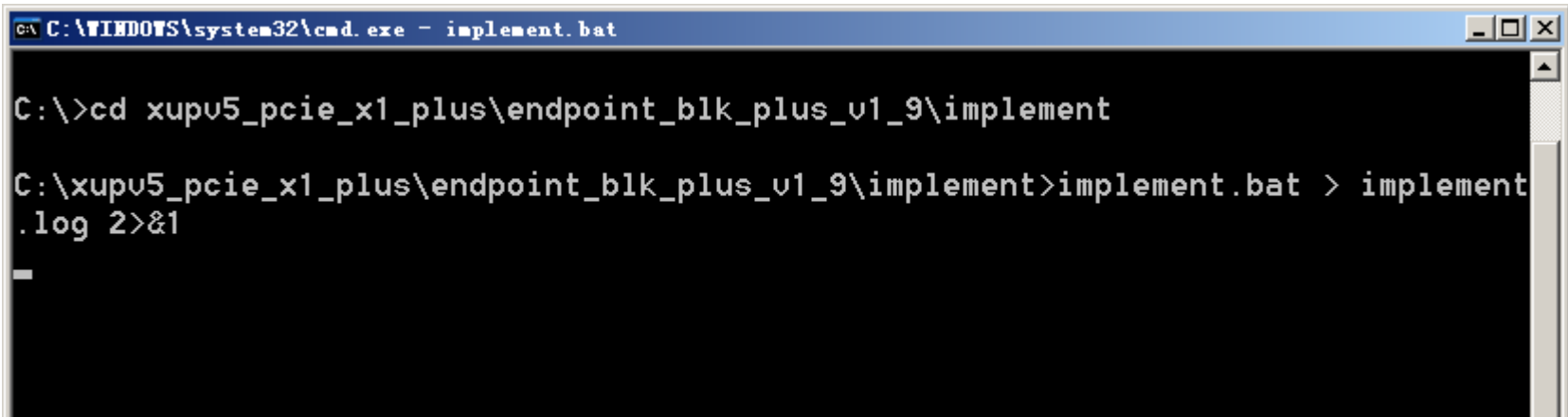
Configure PCIe Core

- The files added are:
 - These two files are required for ACE file generation
 - /implement/make_ace.bat
 - /implement/pcie_ace.cmd
 - Modification to the implementation flow (overwrites existing file)
 - /implement/implement.bat
 - UCF files specific to the XUPV5-LX110T board
 - /example_design/xupv5-lx110t_pcie_x1_plus.ucf



PCIe Core Compilation

- Type these commands in a windows command shell:
 - cd C:\xupv5_pcie_x1_plus\endpoint_blk_plus_v1_9\implement
 - implement.bat > implement.log 2>&1



```
C:\WINDOWS\system32\cmd.exe - implement.bat

C:\>cd xupv5_pcie_x1_plus\endpoint_blk_plus_v1_9\implement

C:\xupv5_pcie_x1_plus\endpoint_blk_plus_v1_9\implement>implement.bat > implement
.log 2>&1

-
```



Generate ACE File

- Type this command in a windows command shell:
 - cd ..
 - make_ace.bat

```
C:\WINDOWS\system32\cmd.exe

C:\Documents and Settings>cd ..

C:\>cd xupu5_pcie_x1_plus\endpoint_blk_plus_v1_9\implement

C:\xupu5_pcie_x1_plus\endpoint_blk_plus_v1_9\implement>implement.bat > implement
.log 2>&1

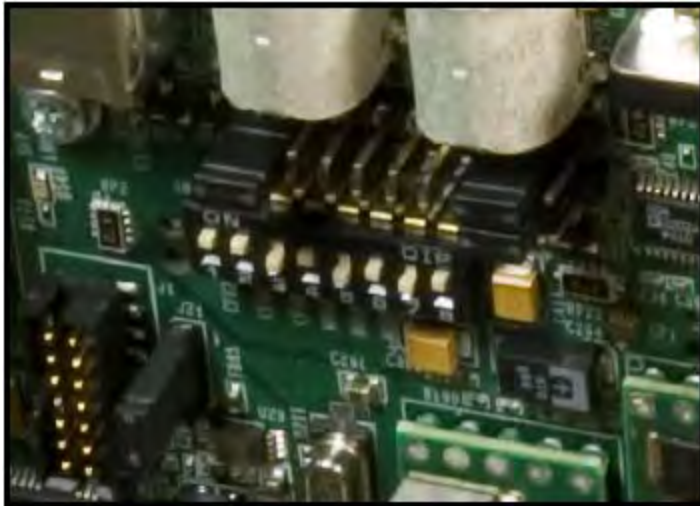
C:\xupu5_pcie_x1_plus\endpoint_blk_plus_v1_9\implement\results>
C:\xupu5_pcie_x1_plus\endpoint_blk_plus_v1_9\implement\results>cd ..

C:\xupu5_pcie_x1_plus\endpoint_blk_plus_v1_9\implement>make_ace.bat
```



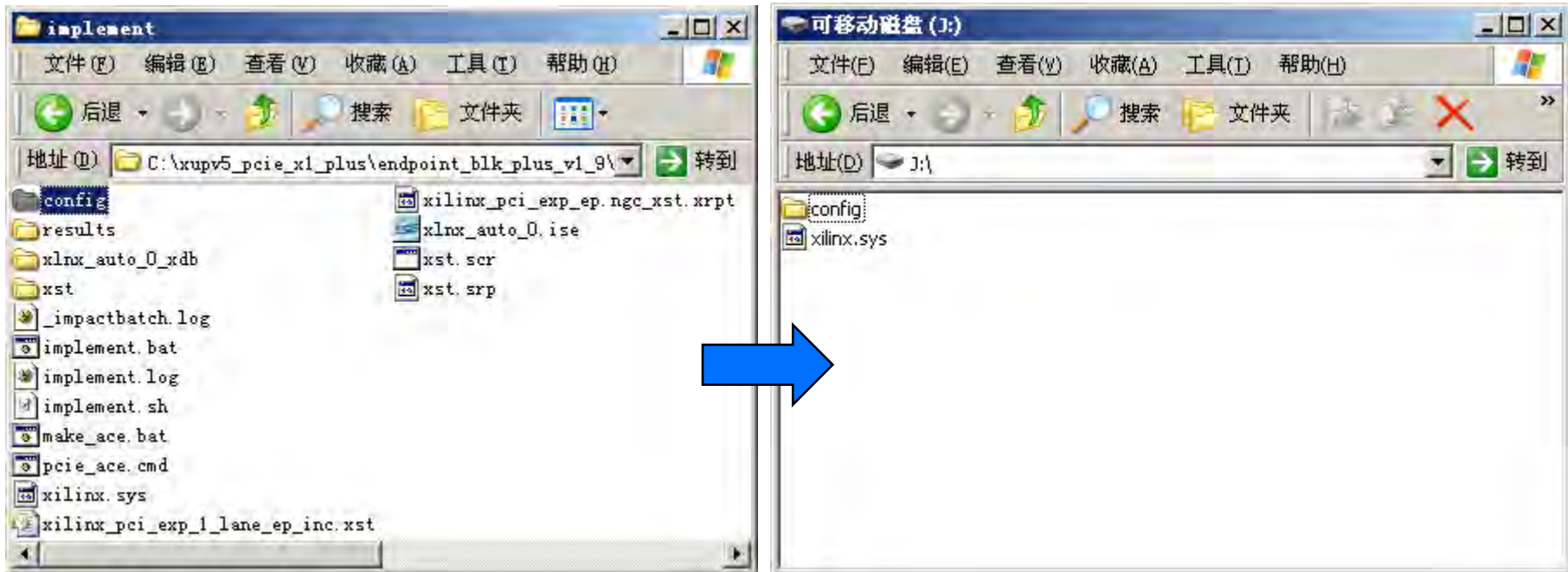
ACE File Execution

- Use a CompactFlash reader to mount the XUPV5-LX110T CompactFlash as a disk drive
- Delete any existing ace files in this <CF Drive>\config\rev6 directory
- Note: rev6 matches the DIP switch settings



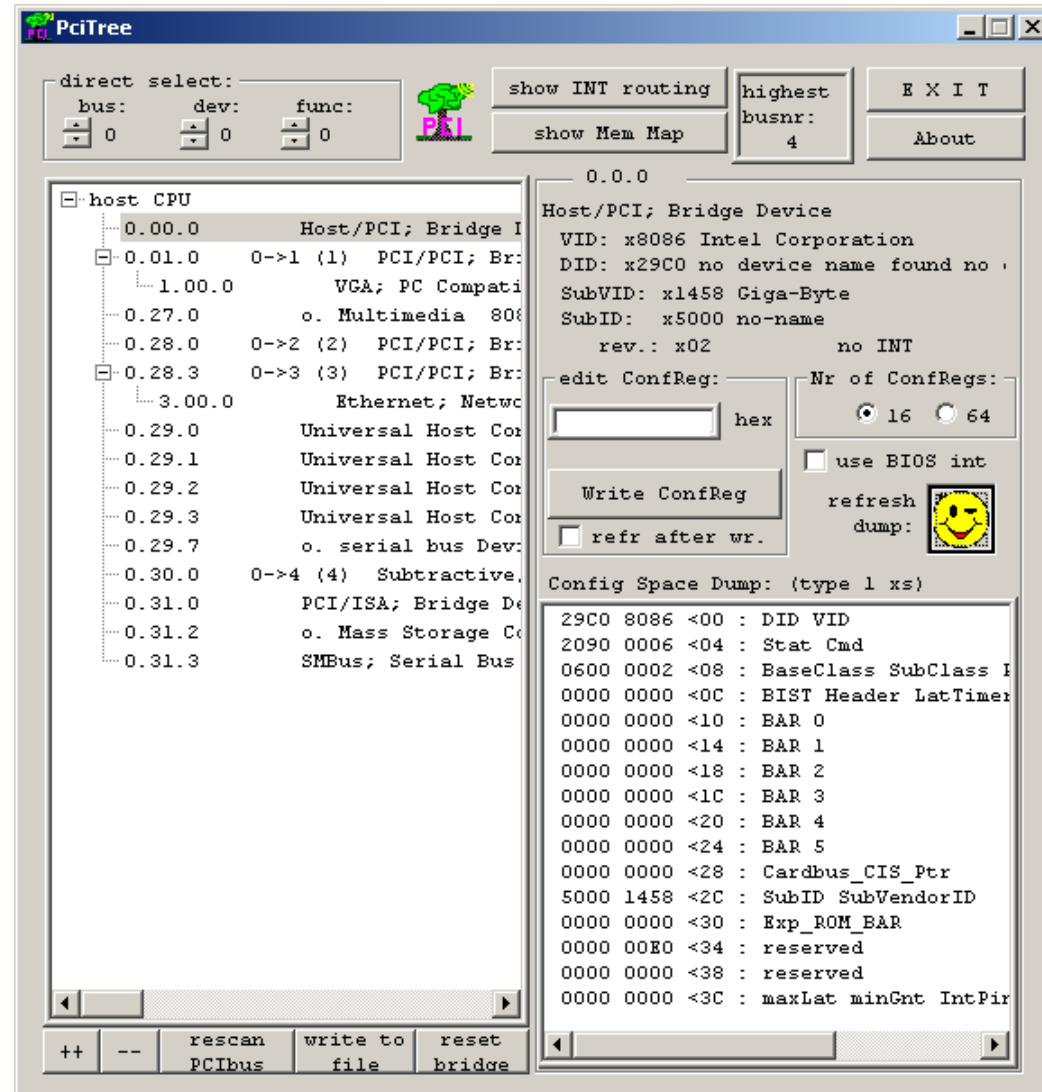
ACE File Execution

- Copy config directory, which contains generated `pcie_blk_plus_top.ace`, to your CompactFlash card



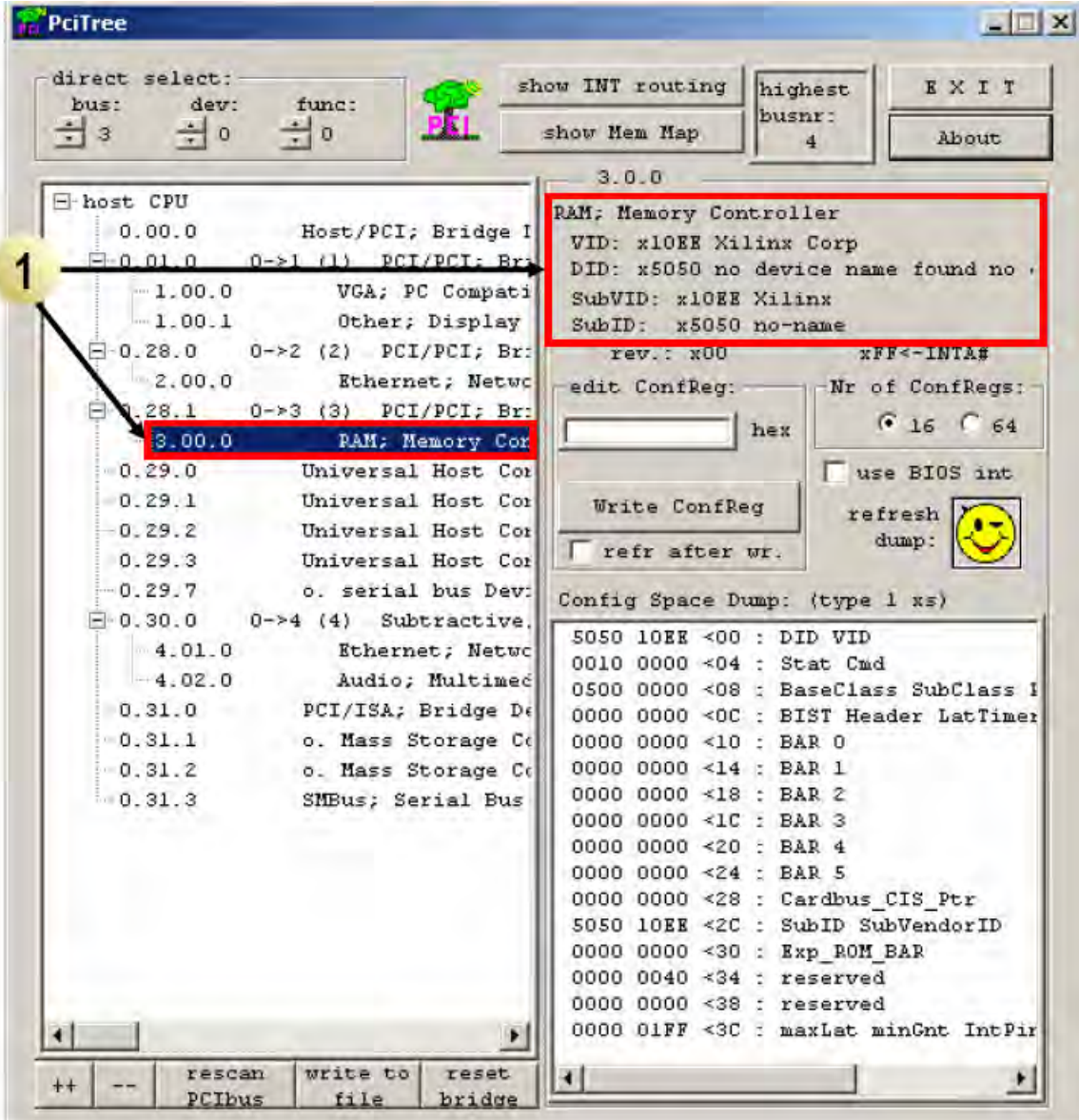
PciTree

- Eject the Compact Flash from your PC, insert it back into the XUPV5-LX110T and power-up the board
- Power on the PC
- Start PciTree



PciTree

- Locate the Xilinx Device
 - Vendor ID 10EE



The screenshot shows the PciTree application window. The main pane displays a tree of PCI devices. A yellow circle with the number '1' is positioned next to the entry '3.00.0 RAM; Memory Controller'. A red box highlights the details for this device, including Vendor ID (VID: x10EE Xilinx Corp) and Device ID (DID: x5050). The Config Space Dump at the bottom shows the device's configuration space, including the Vendor ID field (5050 10EE <2C : SubID SubVendorID).

```
direct select:
bus: 3 dev: 0 func: 0
show INT routing highest busnr: 4
show Mem Map About

3.0.0
RAM; Memory Controller
VID: x10EE Xilinx Corp
DID: x5050 no device name found no
SubVID: x10EE Xilinx
SubID: x5050 no-name
rev.: x00 xFF<-INTA#
edit ConfigReg: hex Nr of ConfigReg: 16 64
Write ConfigReg use BIOS int
refresh dump:
Config Space Dump: (type 1 xs)
5050 10EE <00 : DID VID
0010 0000 <04 : Stat Cmd
0500 0000 <08 : BaseClass SubClass 1
0000 0000 <0C : BIST Header LatTimer
0000 0000 <10 : BAR 0
0000 0000 <14 : BAR 1
0000 0000 <18 : BAR 2
0000 0000 <1C : BAR 3
0000 0000 <20 : BAR 4
0000 0000 <24 : BAR 5
0000 0000 <28 : Cardbus_CIS_Ptr
5050 10EE <2C : SubID SubVendorID
0000 0000 <30 : Exp_ROM_BAR
0000 0040 <34 : reserved
0000 0000 <38 : reserved
0000 01FF <3C : maxLat minCnt IntPir
```



PciTree

- With the Xilinx device selected, double-click on BAR 0

The screenshot shows the PciTree application window. The left pane displays a tree view of PCI devices. The right pane shows detailed information for the selected device, including its configuration space dump.

Device Tree (Left Pane):

- host CPU
 - 0.00.0 Host/PCI; Bridge I
 - 0.01.0 0->1 (1) PCI/PCI; Br
 - 1.00.0 VGA; PC Compati
 - 1.00.1 Other; Display
 - 0.28.0 0->2 (2) PCI/PCI; Br
 - 2.00.0 Ethernet; Netwo
 - 0.28.1 0->3 (3) PCI/PCI; Br
 - 3.00.0 RAM; Memory Cor
 - 0.29.0 Universal Host Cor
 - 0.29.1 Universal Host Cor
 - 0.29.2 Universal Host Cor
 - 0.29.3 Universal Host Cor
 - 0.29.7 o. serial bus Dev:
 - 0.30.0 0->4 (4) Subtractive.
 - 4.01.0 Ethernet; Netwo
 - 4.02.0 Audio; Multimed
 - 0.31.0 PCI/ISA; Bridge De
 - 0.31.1 o. Mass **1** →
 - 0.31.2 o. Mass Storage Co
 - 0.31.3 SMBus; Serial Bus

Device Details (Right Pane):


3.0.0

RAM; Memory Controller

VID: x10EE Xilinx Corp
DID: x5050 no device name found no
SubVID: x10EE Xilinx
SubID: x5050 no-name
rev.: x00 xA<-INTA#

edit ConfigReg: hex Nr of ConfigRegs: 16 64

use BIOS int

refr after wr. refresh 

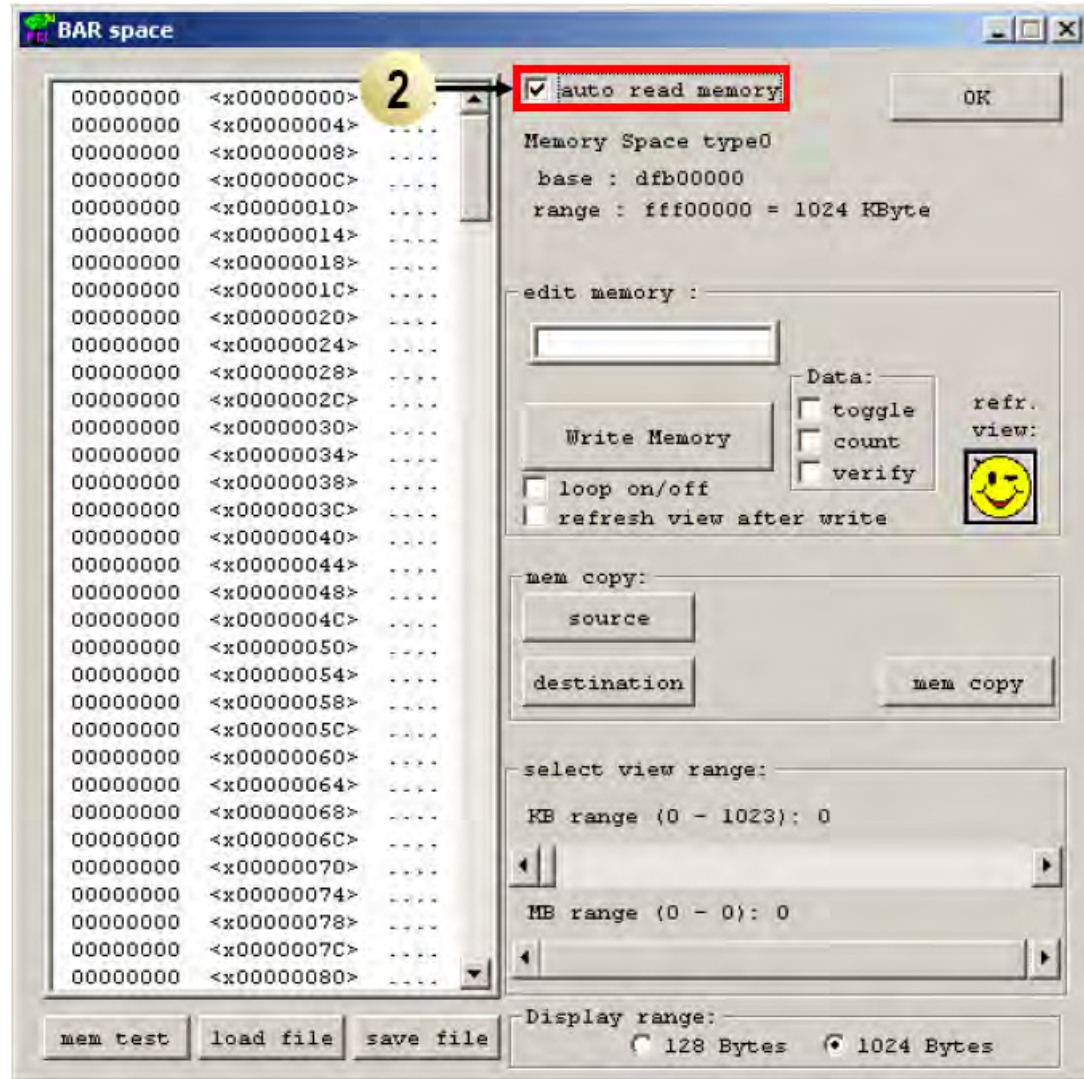
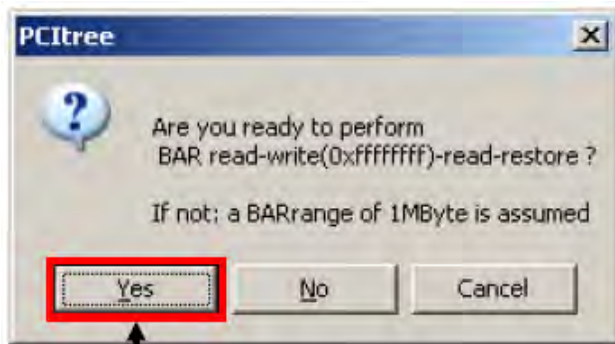
Config Space Dump: (type 1 xs)

```
5050 10EE <00 : DID VID
0010 0107 <04 : Stat Cmd
0500 0000 <08 : BaseClass SubClass I
0000 0010 <0C : BIST Header LatTimer
DFB0 0000 <10 : BAR 0 mem 32bit
0000 0000 <14 : BAR 1
0000 0000 <18 : BAR 2
0000 0000 <1C : BAR 3
0000 0000 <20 : BAR 4
0000 0000 <24 : BAR 5
0000 0000 <28 : Cardbus_CIS_Ptr
5050 10EE <2C : SubID SubVendorID
DFC0 0000 <30 : Exp_ROM_BAR
0000 0040 <34 : reserved
0000 0000 <38 : reserved
0000 010A <3C : maxLat minCnt IntPir
```



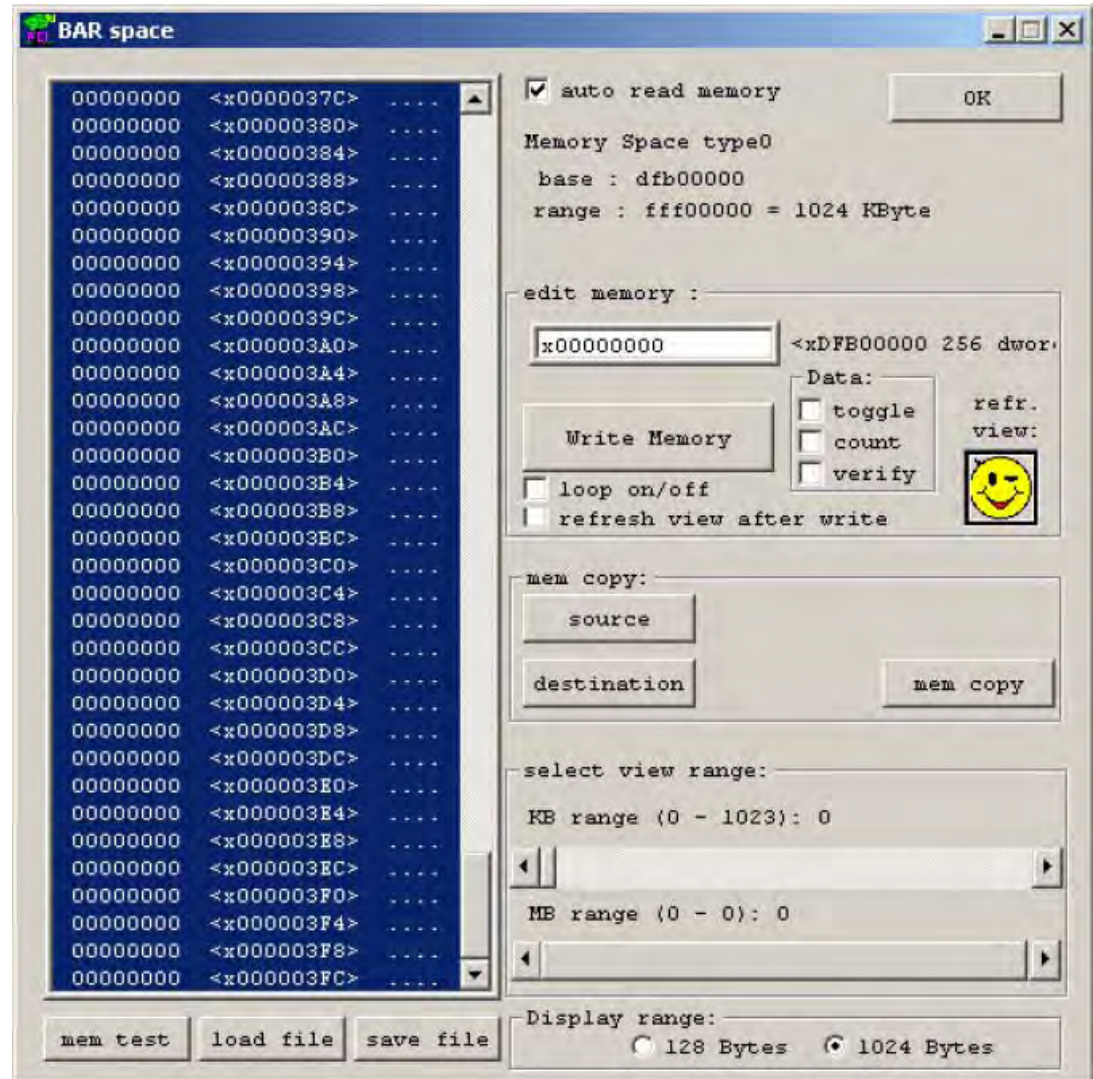
PciTree Bus Viewer

- Click Yes (1)
- Select auto read memory (2)



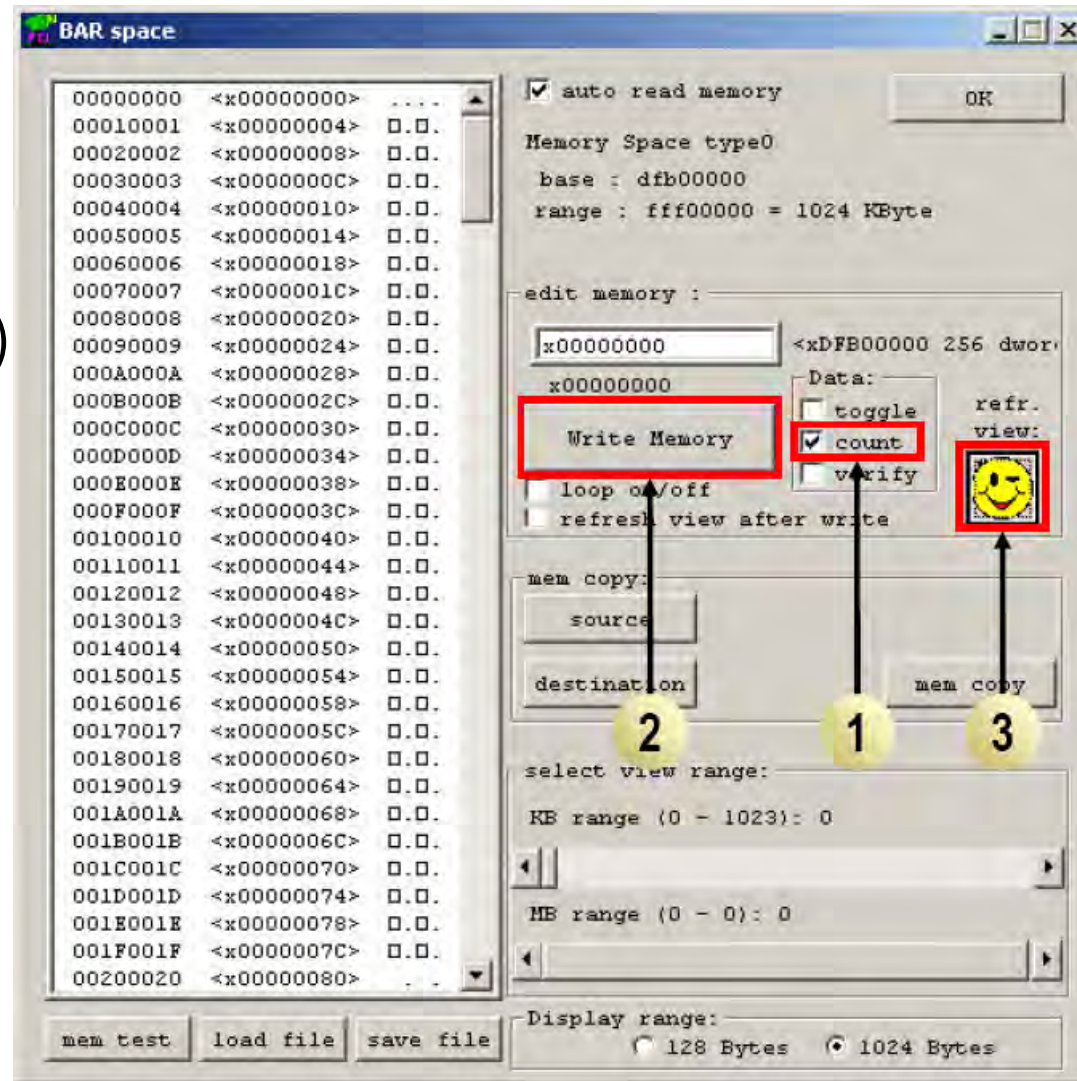
PciTree Bus Viewer

- Click on the first memory location
- Type <Shift-End> to select 1k (256 dwords)



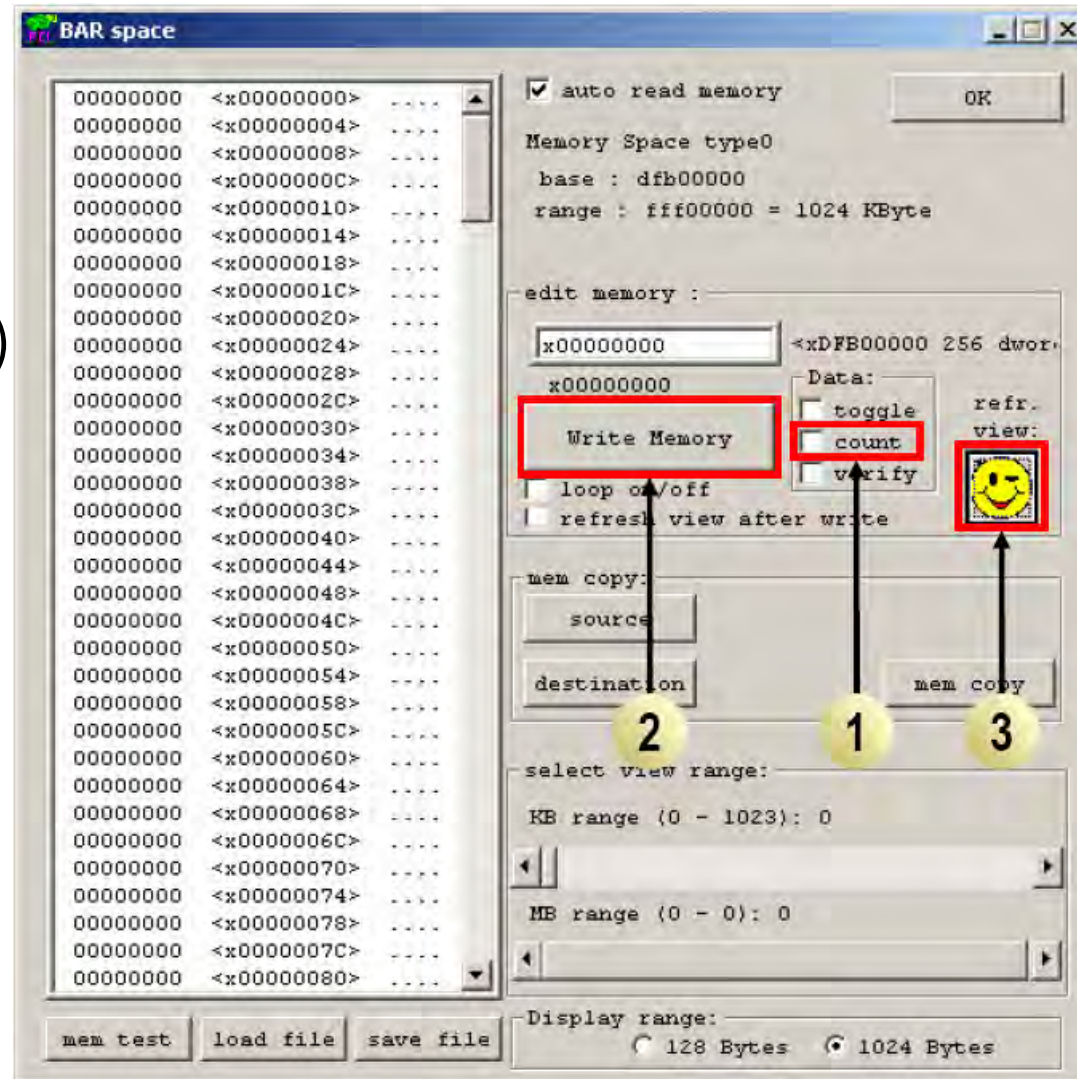
PciTree Bus Viewer

- Write Memory
 - Select count (1)
 - Click Write Memory (2)
 - Click refr view (3)
- View results
 - Counting up to FF



PciTree Bus Viewer

- Restore Memory
 - Deselect count (1)
 - Click Write Memory (2)
 - Click refr view (3)
- Memory is reset to zeros



Documentation

- Virtex-5

- Virtex-5 FPGA User Guide

http://www.xilinx.com/support/documentation/user_guides/ug190.pdf

- Virtex-5 Packaging and Pinout Specification

http://www.xilinx.com/support/documentation/user_guides/ug195.pdf

- Virtex-5 RocketIO

- RocketIO GTP Transceiver User Guide –UG196

http://www.xilinx.com/support/documentation/user_guides/ug196.pdf

- RocketIO GTX Transceiver User Guide –UG198

http://www.xilinx.com/support/documentation/user_guides/ug198.pdf



Documentation

- PCIe
 - LogiCORE Endpoint Block Plus for PCI Express Data Sheet
http://www.xilinx.com/support/documentation/ip_documentation/pcie_blk_plus_ds551.pdf
 - LogiCORE Endpoint Block Plus for PCI Express Designs
http://www.xilinx.com/support/documentation/ip_documentation/pcie_blk_plus_ug341.pdf
 - LogiCORE Endpoint Block Plus Getting Started Guide for PCI Express Designs
http://www.xilinx.com/support/documentation/ip_documentation/pcie_blk_plus_gsg343.pdf
 - Virtex-5 Integrated Endpoint Block User Guide for PCI Express Designs
http://www.xilinx.com/support/documentation/user_guides/ug197.pdf

