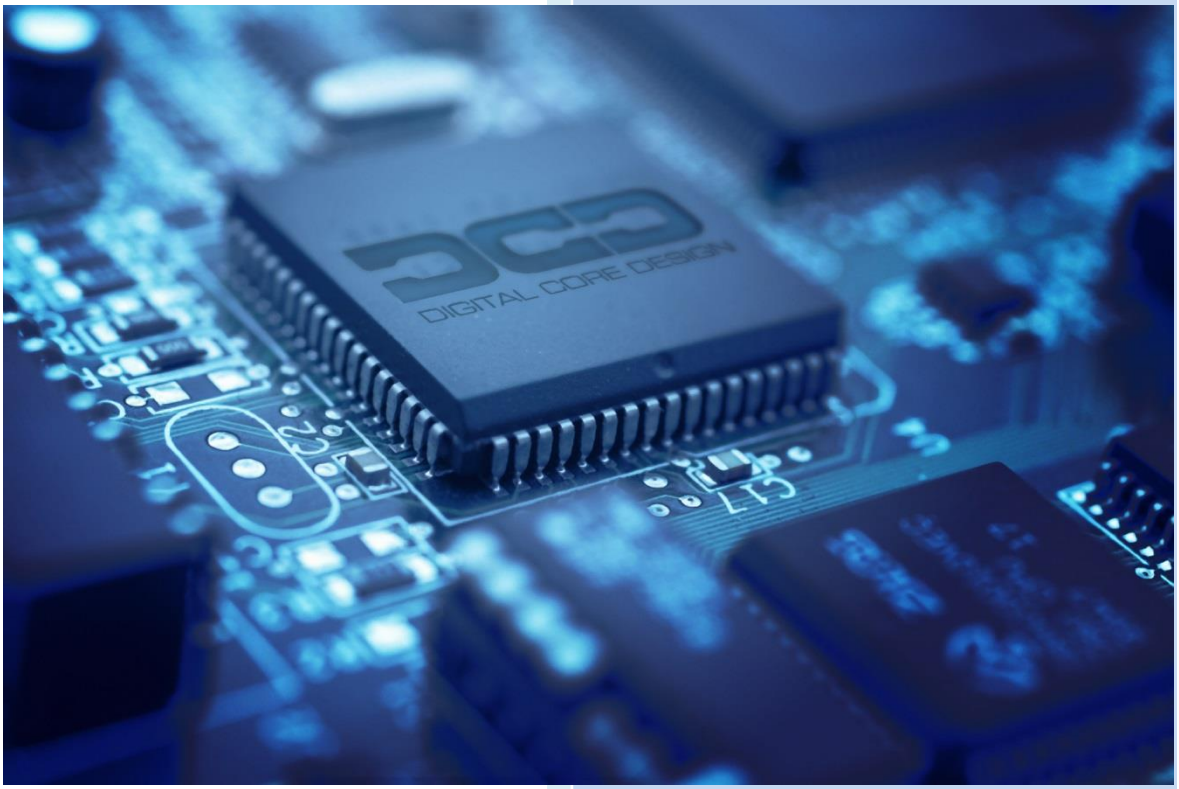
DIGITAL CORE DESIGN

2015

HID Platform IP Core



USB 2.0 HID Design Platform v. 1.10

COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we're designing solutions tailored to your needs.

IP CORE OVERVIEW

The USB 2.0 **HID Design Platform** is a complete, integrated solution, dedicated to a wide range of USB based Human Interface Devices, like mouse, keyboard or pen tablet. The complete HID Design Platform includes:

- DUSB2 peripheral controller, designed to support 12 Mb/s "Full Speed" (FS) and 480 Mb/s "High Speed" (HS) serial data transmission rates
- DP8051XP ultra high performance, speed optimized, fully customizable 8051 8-bit microcontroller with built in DoCD™ debug IP core
- Human Interface Devices software stack optimized for DP8051XP 8-bit CPU
- FPGA board with ready to use, preprogrammed example HID application
- HAD2 – DoCDTM Hardware Assisted Debugger board
- DoCD™ Debug Software
- DoCD™ driver for Keil development software
- DoCD™ driver for IAR development software

MAIN FEATURES

- Full compliance with the USB 2.0 specification
- Full-speed 12 Mbps operation
- High-speed 480 Mbps operation
- Supports UTMI Transceiver Macrocell Interface
- Suspend and resume power management functions
- 100% software compatible with industry standard 8051
- Up to 256 bytes of internal (on-chip) Data Memory
- Up to 64K bytes of internal (on-chip) or external (off-chip) Program Memory
- Up to 16M bytes of external (off-chip) Data Memory
- User programmable Program Memory Wait States solution for wide range of memories speed
- User programmable External Data Memory Wait States solution for wide range of memories speed
- Fully synthesizable, static synchronous design with positive edge clocking and no internal tri-states
- Scan test ready

DELIVERABLES

- Source code:
  - VHDL Source Code or/and
  - VERILOG Source Code or/and
  - Encrypted, or plain text EDIF
- VHDL & VERILOG test bench environment
  - Active-HDL automatic simulation macros
  - ModelSim automatic simulation macros
  - Tests with reference responses
- Technical documentation
  - Installation notes
  - HDL core specification
  - Datasheet
- Synthesis scripts
- Example application
- Technical support
  - IP Core implementation support
  - 3 months maintenance
    - Delivery of the IP Core and documentation updates, minor and major versions changes
    - Phone & email support

LICENSING

Comprehensible and clearly defined licensing methods **without royalty-per-chip fees** make use of our IP Cores easy and simple.

Single-Site license option – dedicated to small and middle sized companies, which run their business in one place.

Multi-Site license option – dedicated to corporate customers, who operate at several locations. The licensed product can be used in selected company branches.

In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. The license is royalty-per-chip free. There are no restrictions regarding the time of use.

There are two formats of the delivered IP Core:

- VHDL or Verilog RTL synthesizable source code called HDL Source code
- FPGA EDIF/NGO/NGD/QXP/VQM called Netlist

UNITS SUMMARY

UTMI Interface – The UTMI interface is clocked by utmiclk clock and manages communication with USB 2.0 Transceiver Macrocell. It is responsible for reset detection, speed handshake, token, data and handshake packet reception and transmission.

CPU Interface – The CPU interface module is clocked by cpuclk clock and manages communication with DP8051XP CPU. In this module DUSB2 core configuration and status registers are being located.

SRAM Interface – The SRAM interface module manages communication with Synchronous Random Access Memory. It generates address, read and write signals for the SRAM memory and buffers data bytes during the FIFO read and write operations.

EP0 endpoint –The EP0 control endpoint is Special bidirectional endpoint used for device configuration. Allows generic USB control and status access.

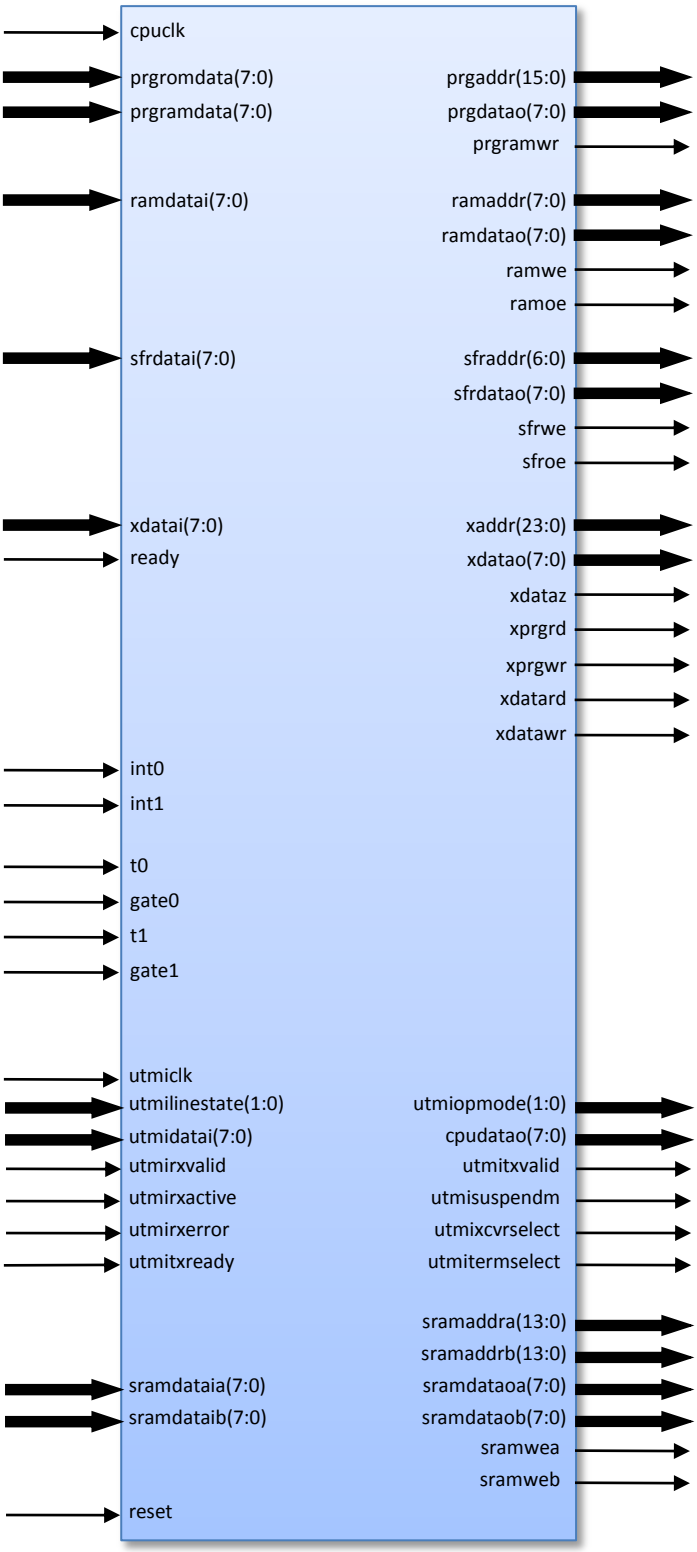
EP1 & EP2 endpoints – The EP1 and EP2 data endpoints are unidirectional, configurable endpoints, used for application specific data transmission.

DP8051XP CPU – Ultra high performance, speed optimized 8-bit embedded controller, 100% software compatible with industry standard 8051

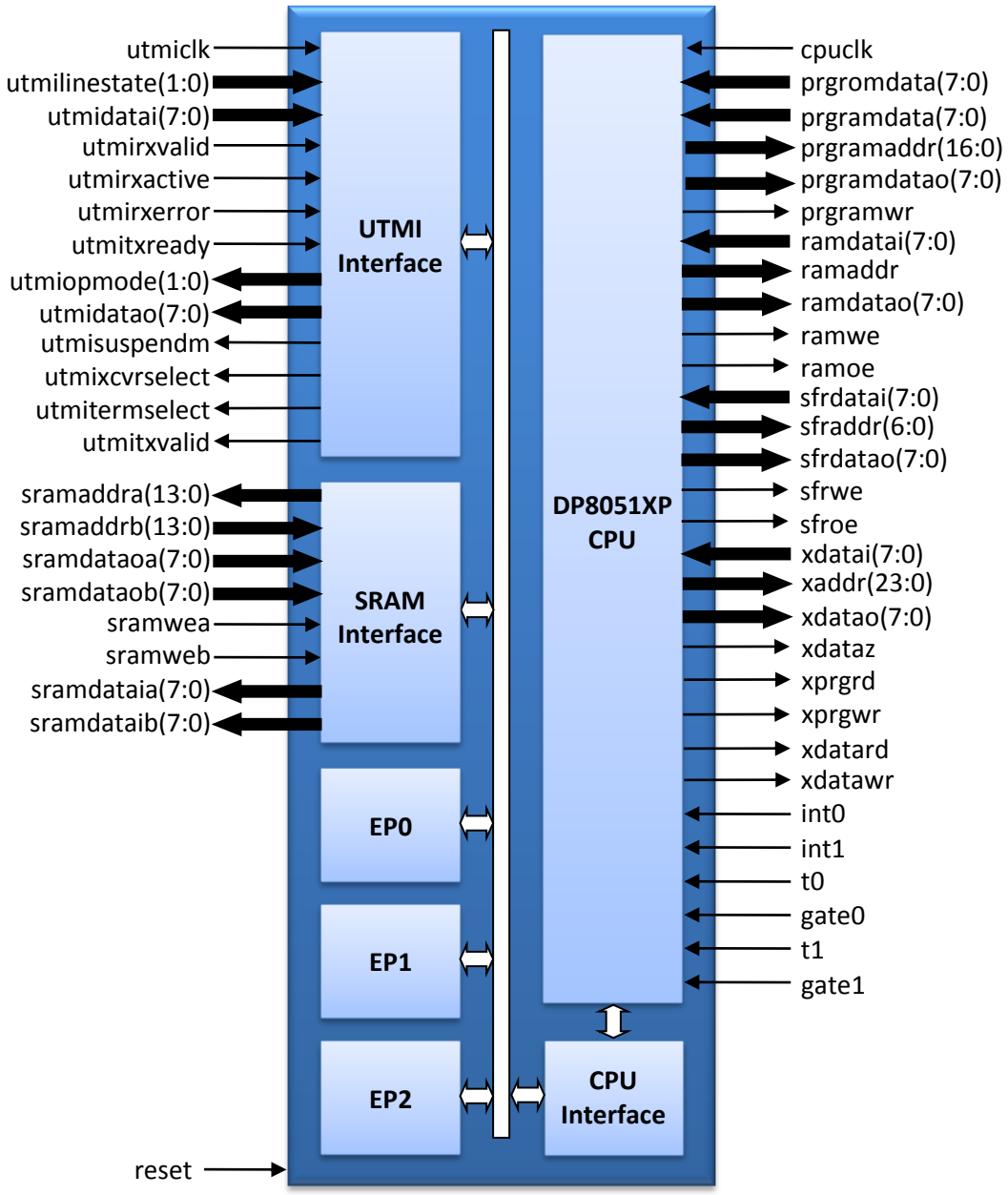
PINS DESCRIPTION

PIN	TYPE	DESCRIPTION
reset	input	Global reset
utmiclk	input	USB clock
utmilinestate(1:0)	input	USB line state
utmidatai(7:0)	input	USB parallel data input bus
utmirxvalid	input	USB receive valid
utmirxactive	input	USB receive active
utmirxerror	input	USB receive error
utmitxready	input	USB transmit ready
sramdataia(7:0)	input	SRAM port A data input bus
sramdataib(7:0)	input	SRAM port B data input bus
cpuclk	input	CPU clock
prgramdata[7:0]	input	Data bus from internal RAM program memory
prgromdata[7:0]	input	Data bus from internal ROM progogram memory
ramdatai[7:0]	input	Data bus from internal data memory
sfrdatai[7:0]	input	Data bus from user SFR's
xdatai[7:0]	input	Data bus from external memories
int0	input	External interrupt 0
int1	input	External interrupt 1
t0	input	Timer 0 input
gate0	input	Timer 0 gate input
t1	input	Timer 1 input
gate1	input	Timer 1 gate input
utmiopmode(1:0)	output	USB operational mode
utmidatao(7:0)	output	USB parallel data output bus
utmisuspendm	output	USB suspend
utmixcvrselect	output	USB transceiver select
utmitermselect	output	USB termination select
utmitxvalid	output	USB transmit valid
sramaddra(13:0)	output	SRAM port A address bus
sramaddrb(13:0)	output	SRAM port B address bus
sramdataoa(7:0)	output	SRAM port A data output bus
sramdataob(7:0)	output	SRAM port B data output bus
sramwea	output	SRAM port A write enable
sramweb	output	SRAM port B write enable
prgaddr[15:0]	output	Internal program memory address bus
prgdatao[7:0]	output	Data bus for internal program memory
prgramwr	output	Internal program memory write
ramaddr[7:0]	output	Internal Data Memory address bus
ramdatao[7:0]	output	Data bus for internal data memory
ramoe	output	Internal data memory output enable
ramwe	output	Internal data memory write enable
sfraddr[6:0]	output	Address bus for user SFR's
sfrdatao[7:0]	output	Data bus for user SFR's
sfroe	output	User SFR's output enable
sfrwe	output	User SFR's write enable
xaddr[23:0]	output	Address bus for external memories
xdatao[7:0]	output	Data bus for external memories
xdataz	output	Turn xdata bus into 'Z' state
xprgrd	output	External program memory read
xprgwr	output	External program memory write
xdatard	output	External data memory read
xdatawr	output	External data memory write

SYMBOL



BLOCK DIAGRAM



PERFORMANCE

The following tables give a survey about the Core area and performance in Programmable Logic Devices after Place & Route.

Device	Speed grade	cpuclk F_{max}	utmiclk F_{max}
SPARTAN-III	-5	50 MHz	>100 MHz
SPARTAN-IIIE	-5	60 MHz	>100 MHz
VIRTEX-4	-12	75 MHz	>100 MHz
VIRTEX-5	-3	90 MHz	>100 MHz

Core performance in XILINX® devices

An area utilized by a complete, integrated USB 2.0 HID Design Platform in vendor specific technologies is summarized in the following table.

Component	Area [Slices]	[FFs]
CPU interface	225	170
UTMI interface	265	230
SRAM interface	115	95
EP0 endpoint	150	140
EP1 endpoint	160	155
EP2 endpoint	160	155
DP8051XP CPU	1230	395
DoCD™ debug IP core	375	270
Total area	**2680**	**1610**

Core components area utilization in XILINX® devices except VIRTEX-5 family

Component	Area [Slices]	[FFs]
CPU interface	120	170
UTMI interface	145	230
SRAM interface	65	95
EP0 endpoint	80	140
EP1 endpoint	85	155
EP2 endpoint	85	155
DP8051XP CPU	595	395
DoCD™ debug IP core	230	270
Total area	**1405**	**1610**

Core components area utilization in XILINX® VIRTEX-5 devices

CONTACT

For any modifications or special requests, please contact Digital Core Design or local distributors.

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