Synchronization of Signal Processing in Multiple RF Data Converter Subsystems

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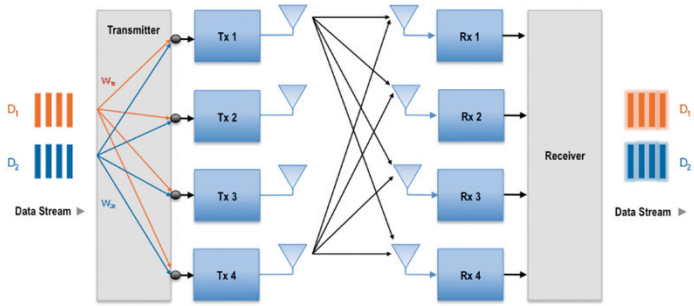
Summary

Synchronization requirements in emerging RF applications are challenging due to the increasing number of antennas used. The majority of new radio applications use MIMO with OFDM encoding to increase the capacity of the radio links. MIMO, when coupled with direct RF conversion and digital signal processing, requires advanced processing to preserve the phase coherency in the digital RF transceiver design.

Introduction

Multi-channel applications targeting very large scale systems (RADAR, electronic warfare, satellite communication, and massive MIMO) are now combining multiple input multiple output (MIMO), beam-forming, and controlled latencies with other classical requirements of RF channel design such as linearity, noise and spectral purity. This shift in technology is occurring simultaneously to the move to the RF direct conversion to enable the level of integration required. The radio transmitter and radio receiver architecture, a MIMO system will trigger a requirement to distinguish multiple data streams, the following figure illustrates a typical MIMO system in which the channel alignment is critical.

Figure 1: **Typical MIMO Architecture**



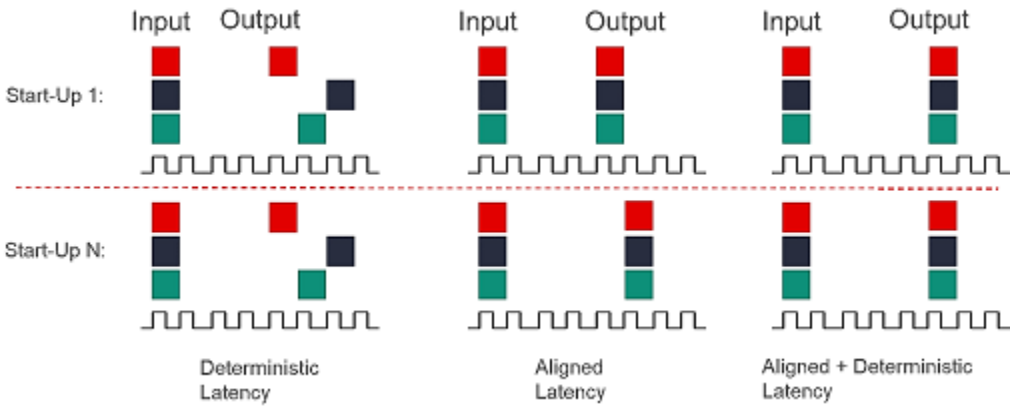
Most of the technologies used to encode and decode the information are passing through the radio signal requires RF path alignment to enable the MIMO transceiver system. This requirement becomes mandatory and critical when the RF subsystem enables beam-forming. Therefore, latency control from user data to the antenna becomes a critical requirement and is linked to the design system RF clocking requirements using direct RF conversion. The application may have different requirements:

- The latency alignment– The difference in latency between channels.

- The latency determinism– The total latency for each channel is consistent between start-ups of the full system.

The following figure illustrates the concepts of latency alignment and latency determinism.

Figure 2: **Alignment and Deterministic Latency**



In any systems with multiple independent RF converters and clocking structures, there are several potential sources of latency uncertainty. Matching these latencies is critical, but also challenging and can consume a lot of power in a large system using multiple discrete converters. Discrete converters have standardized the use of the JESD204B SYSREF scheme for synchronization. Similarly, the Zynq® UltraScale+™ RFSoC has implemented a complementary, simplified scheme using SYSREF signal, which is a shared signal that defines a common timing reference.

The integration of the RF data converters in the Zynq UltraScale+ RFSoC results in the elimination of the serial transceiver links for RF digital communication that typically consume power and add latency. However, to provide a flexible clocking and number of data words for the PL (Programmable Logic) design, each RF-ADC and RF-DAC digital signal processing block incorporates independent gearbox FIFOs. These FIFOs allow data to be transferred between the PL clock domain and the RF converter sample clock domain which can result in a non-deterministic latency across the async FIFO, which causes the uncertainty in latency between different tiles. This latency is measured and corrected using the Multi-Tile Synchronization (MTS) feature.

Basic Theory

The Zynq UltraScale+ RFSoC achieves high accuracy synchronization across multiple channels and chips via MTS.

In comparison with the JESD-204B/C standard, the MTS benefits from the integration of converters and FPGA in one chip, which gives the alignment accuracy tolerance significant better than ±T1 (± one converter sampling clock period) without complex 204B/C transceiver and synchronizing process. The MTS also supports deterministic latency with relaxed clock scheme in the system using a single API call.

It is possible to achieve significantly better alignment than ±T1 by optimizing system design including board design. Refer to *UltraScale Architecture PCB Design User Guide* (UG583) for specific board design recommendations. The following sections detail the various design aspects to which users should pay close attention to achieve optimized synchronization performance.

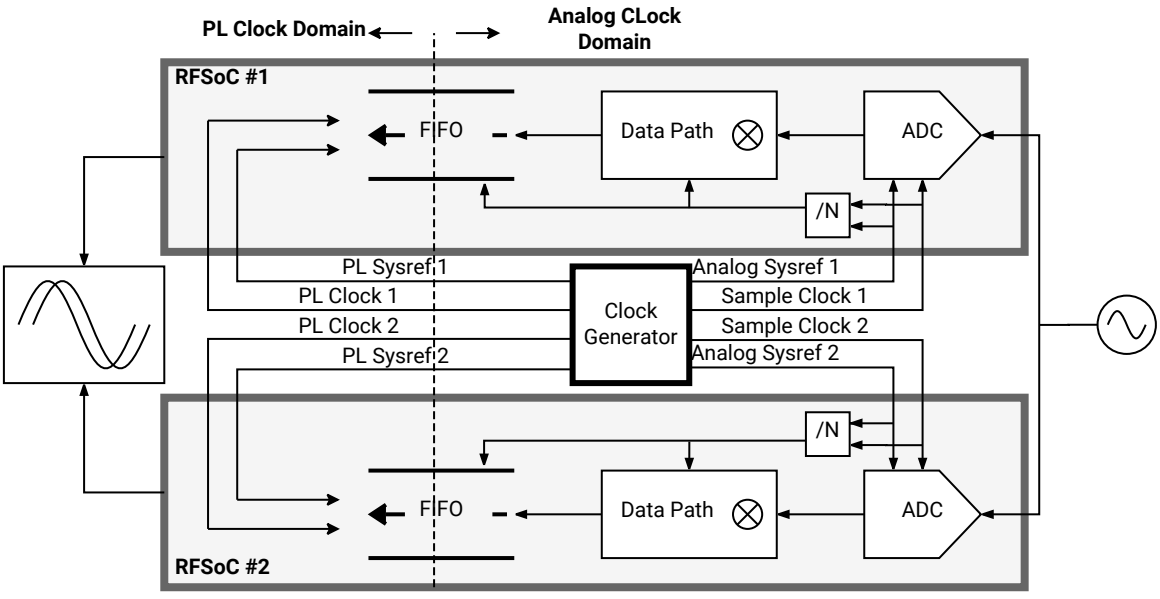
Synchronization of a system using multiple RFDC sub-systems with one or several devices requires a common clock synchronization through the set of sub-systems. Where several synthesizers are used to supply the reference clock to the RFDC, clock synchronization is mandatory, otherwise the random frequency drift from the different sources will be unpredictable. Sampling clocks from different PLLs are acceptable, but these PLLs must be frequency locked and phased aligned.

When frequency drift among a set of clocks of RFDC subsystem is no longer a concern, the MTS feature of Zynq UltraScale+ RFSoC will handle alignment of the propagation delay from converters to the programmable logic and vice versa. MTS aligns all synchronous blocks within the tiles, then aligns the dual clock FIFO interface between the PL and RFDC through pointer adjustments.

In addition to the sampling clocks used in RFDC subsystem clock domains and PL clocks used in PL domains, the MTS also relies on time base references analog_sysref (tied to RFDC clock domains) and PL_sysref (tied to PL clock domain) to perform alignment. These low jitter signals are used to measure propagation delay from a common and precise time reference in the 2 different clock domains. They are also used to trigger sub-system events linked to phase alignment requirements.

In summary, the MTS algorithm achieves alignments across multiple RFDC subsystems from one or more RFSoCs using a measure and adjust mechanism. The measure and adjust mechanism relies on the analog_sysref and PL_sysref timing reference. As an example, the following figure shows an overview of the MTS across two chips.

Figure 3: **Multiple Tile Synchronization Across Two Chips**



There are 2 RFSoCs and one ADC channel for each chip illustrated in Figure 3, however, there are up to 16 ADCs and 16 DACs in a single chip. There is no limitation to number of RFSoCs or converter tiles from the MTS mechanism, the similar architecture can be expanded to include more RFSoC chips in the system.

Note: The alignment mechanism from the MTS is the same for several tiles inside one RFSoC or several tiles from several RFSoCs.

Digital Datapath

The digital datapath includes the whole digital signal processing between the PL and the analog RF converters. The Zynq UltraScale+ RFSoC offers a specific set of tiles to enable multiple RFDC channels in a device. Each tile consists of multiple channels. All channels within a tile are intrinsically synchronized by design, but not deterministic from reset to reset. MTS will be needed to achieve this. Care should be taken to ensure the NCOs are reset appropriately when using the NCO in multiple channels in a tile.

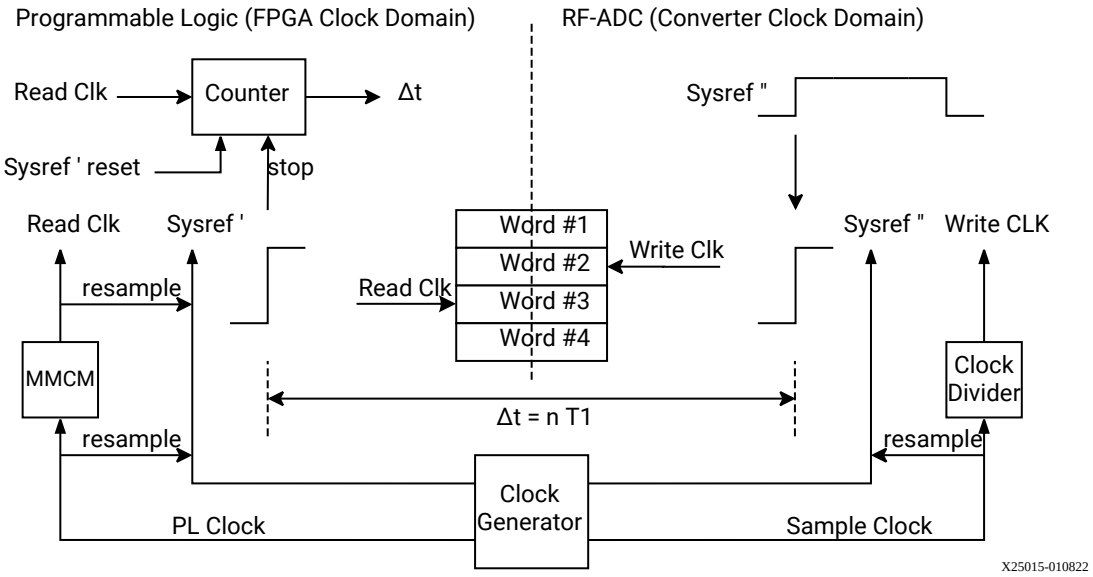
The MTS mechanism works the same way across multiple tiles or multiple chips. All chips will align their sample stream on the rising edge of their own analog_sysref signal when the MTS API is called. The rising edge of each individual analog_sysref can also be used as a trigger to dynamically update the NCO or QMC in the digital datapath on the fly. As an example, the QMC might change the signal phase and this updated phase can be applied at the same time across multiple tiles using the analog_sysref as a trigger.

Dual Clock FIFO

The FIFOs are located between the RF converters (Analog converters together with RF Datapath) and the PL to buffer data and transfer between the PL and RFDC clock domains. Because the read and write clocks are from different clock domains, these clocks can have a different phase relationship over power on/off cycles. We must distinguish between the RFDC clock domain and the PL clock domain.

The following figure shows how MTS evaluates the misalignment between FIFOs. The ADC channel is used as example and similar operation is performed for DAC with the opposite signal flow direction.

Figure 4: **MTS Synchronization across RF data converter to PL clock domains**



The propagation delay between FIFOs is uncertain after initialization, this is normal for most dual clock FIFOs. The MTS mechanism measures the propagation delay of each FIFO and compensates for the difference between them. This operation will not only align all FIFO delays, but also ensures deterministic latency across FIFOs over multiple power cycles if users apply a specific latency value with margin as explained in Zynq UltraScale+ RFSoC product guide. The resolution of this compensation is one sampling clock period (T1).

By using the FIFO measurement and compensation procedure we know that the absolute alignment between each of these clock groups (analog_sysref, PL_sysref, PL_clock and sample clock) are not critical, while the alignment within each clock groups are critical for synchronization across multiple tiles or chips:

- Alignment of all PL_sysref across chips
- Alignment of all analog_sysref across chips
- Alignment of all sampling clock across chips
- Alignment of all PL clock across chips

Board design should make sure the clock source is stable to keep a constant phase relationship between them over time, this makes sure a safe and stable capturing of analog_sysref and PL_sysref by sample clock and PL_clock respectively. When MTS is used on a single chip, there are no PCB trace alignment constraints on these four key signals used to manage timing references. But the constant phase relationship within each clock domain is still necessary.

For strict deterministic latency over reset to reset cycles, the following requirement must be met:

- Constant phase relationship between analog_sysref and PL_sysref supplied to the device over reset to reset cycles.

Algorithm Illustration

For any RFSoC, MTS will send the rising edge of analog_sysref across the FIFO from the ADC tile to PL or vice versa for the DAC. A counter stops once this rising edge is detected in PL. This counter is reset by each rising edge of the PL_sysref in PL and incremented by each word from FIFO. Once the counter stops, the counter value represents the relative propagation latency of this FIFO. Running the same measurement for all selected tiles in the device, MTS gets the FIFO mismatch of all tiles and then aligns them by adding additional delays to ensure that the delay through each FIFO matches the largest measured delay. When the system contains several RFSoCs, the system just needs to call the MTS function for each device.

Users should note that the measured FIFO latency is a relative value and not representative of the physical propagation delay across FIFO, because the measured delay is depending on when the counter is reset with reference to the rising edge of analog_sysref.

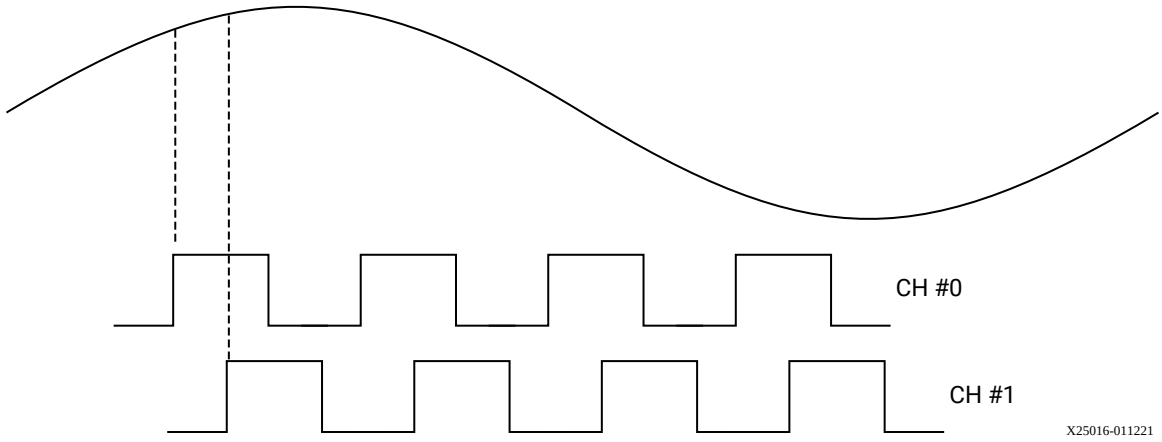
Sources of Misalignment

Misalignment of Sampling Clock

The sampling clock is the time base of RFDC time domain. Data passes through each digital function block in parallel or sequential based on the sample clock edge. In addition to this, the analog_sysref signal is re-sampled by the sampling clock. All of these sampling needs impact MTS performance. As there are so many aspects of the RFDC impacted by sampling clock misalignment and the interactions between them, it's difficult to evaluate the exact misalignment caused by sample clock mismatch. However, as a continuous clock, the maximum misalignment of sample clocks is no more than ±T1/2 in the RF digital system.

With exception to the above, the misalignment on converter sampling clock also generates offsets in sampling, and this error won't be identified and corrected by MTS because it's outside of the MTS loop. As a result of this, the user must be careful when undertaking both measurements and design. The following figure illustrates the sampling misalignment.

Figure 5: **Misalignment of Sampling Clock Example**



Align the sampling clocks for the best possible synchronization in a system.

Misalignment due to On-chip RF PLLs

Each tile in RFSoC has the option to use its own RF PLL to generate the RF converter sampling clock on-chip. These on-chip RF PLLs help to avoid high frequency sample clocks routing on board. When enabled, MTS will align the output divider (divider after VCO in a PLL) of each on-chip PLL at the rising edge of analog_sysref, hence align the sample clocks. From the PLL theory, we know the output phase keeps constant relationship with its reference. To keep the sample clock well aligned, the input reference clocks to each pll must be aligned to each other.

Even if the output divider of the RF PLLs will be well aligned by MTS, the VCOs may run at small different phases in the different device samples, voltage and temperature environment. The effect is expected to be small compared to a full period of sampling clock but need to be considered when high accuracy alignment is required.

In third generation of Zynq UltraScale+ RFSoC, the new on-chip clock forwarding feature can distribute the sampling clock from an external synthesizer or from one On-chip RF PLL output to a set of tiles. This can eliminate the misalignment of either multiple external synthesizers or multiple internal PLLs across tiles in a single device and can simplify the clock distribution PCB layout.

For multiple chips alignment, it is required to well align the sampling clocks for each targeted chip and clock distribution feature to minimize this misalignment.

Misalignment due to External Clock Generator

A clock generator has skews between each of its clock outputs typically. The misalignment caused by clock generators can not be identified or corrected by MTS process in general which should be calibrated by the clock generator itself or at system level. For example, the output skew between two clock outputs is ±30ps, and the two output frequencies are 250MHz (T1=4ns). This will generate a phase misalignment around ±2.7degree.

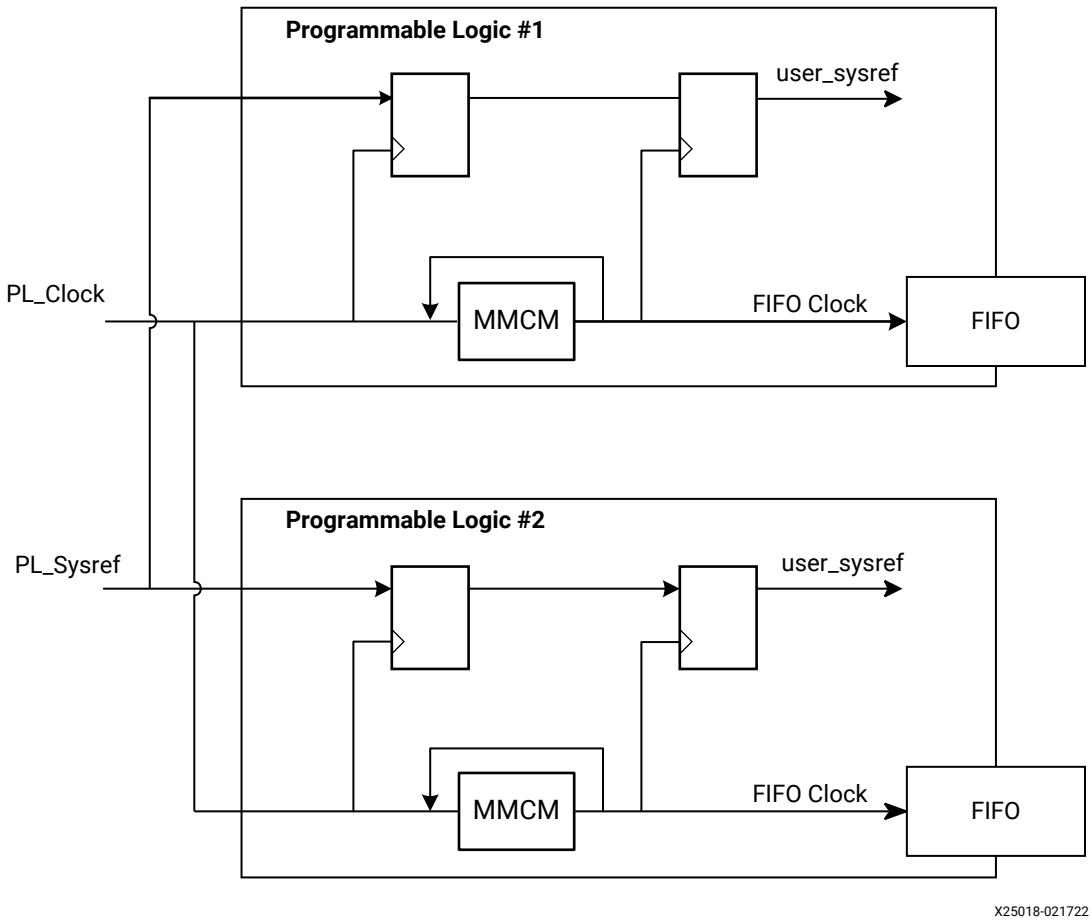
In system design, the clock to each chip may be from the same clock generator, clock buffer or directly distributed from clock amplifier. In any case, the review of the clock paths skew is required to achieve high accuracy alignment in the whole system.

Misalignment in Programmable Logic

PL_clock and PL_sysref are the key clocks in FPGA side for synchronization.

The following figure shows a brief implementation of MTS related clocks in programmable logic.

Figure 6: **MTS Related Clocks in Programmable Logic**



The PL SYSREF must be sampled by the PL clock to make it synchronous to the PL clock domain. We can consider the PL SYSREF and the User SYSREF to be conceptually the same. This doesn't affect the measurement theory outlined above.

In most real applications, the clock used in PL domain to interface with RFDC dual clock FIFO is different from the PL_clock. Hence MMCM in PL domain is used to synthesize the wanted PL_clock driving the FIFO clocks for interfacing RFDC sub-system.

As indicated in Zynq UltraScale+ RFSoC RFDC product guide [Ref 1] the FIFO clock rates of both ADC and DAC must be common multiple of PL_sysref and PL_Clock. For synchronization across multiple chips, an additional requirement is MMCM use to drive FIFO clock must enable external 0-delay mode, this helps to align the FIFO clocks across multiple chips.

For example, if the desired FIFO clocks are 300MHz in a system multiple MMCM will generate phase aligned outputs from a PL_clock of 100MHz, but may generate misaligned 300MHz when the PL_clock is 200MHz. MTS is not aware of this misalignment.

Signal Trace Mismatch

The misalignment of input (for RF-ADC) or output (for RF DAC) analog signal traces can't be taken into account and compensated by MTS mechanism. However, the misalignment caused by the PCB trace mismatch can be estimated with the following formula using strip line design.

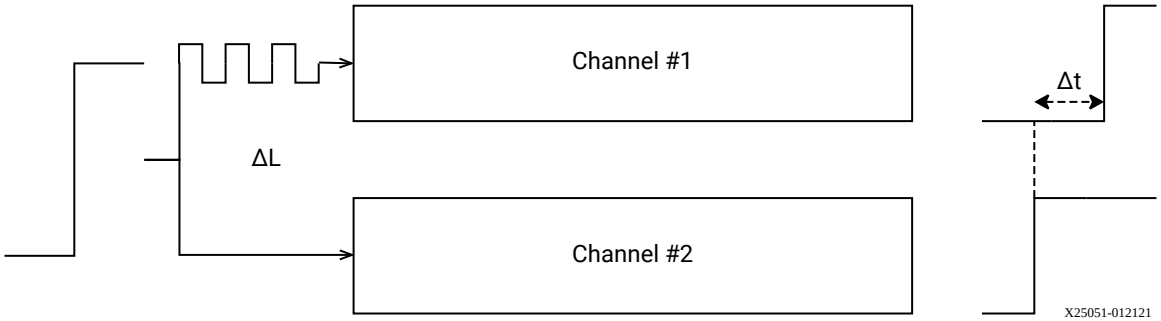
$$\Delta T_{misalignment}(time) = \frac{\Delta L}{c\ in\ dielectric} = \frac{\Delta L \times \sqrt{E_r}}{c}$$

where:

- c is the velocity of electromagnetic field in vacuum.
- Er is the relative dielectric constant of PCB material.

The following figure illustrates the trace mismatch in the signal path.

Figure 7: **Trace Mismatch in the Signal Path**



For example, on a PCB with the relative dielectric constant of 4, assuming the mismatch of two traces is 100mil, the misalignment in time is around 16.9ps, for the carrier frequency of 3.5GHz, which lead to a misalignment of 21.35° in degree.

If the digital up/down conversion is enabled in the data path, the misalignment in degree doesn't change and the Δt should be calculated based on the Δϕ (radian difference) of IF (intermediate frequency). This can be derived from the following formula (down conversion for example):

$$e^{j\omega_{RF}t+\Delta\phi} \cdot e^{-j\omega_{NCO}t} = e^{j(\omega_{RF}-\omega_{NCO})t+\Delta\phi} = e^{j\omega_{IF}t+\Delta\phi}$$

$$\Delta t(at\ IF\ or\ Baseband) = \frac{\Delta\phi}{2\pi} \cdot T_{IF}$$

Where the Δϕ is the misalignment in radians at carrier frequency.

Trace mismatch must be controlled by the PCB designer because MTS can only provides digital alignment in the tile and programmable logic. Trace length compensation to achieve the best possible alignment at the system level must be handled primarily by the PCB design. There is scope to calibrate out any residual alignment in channel using DSP blocks in the Programmable Logic.

Deterministic Latency

The latency determinism requires a fixed delay across channels and chips over reset to reset cycles.

The Zynq UltraScale+ RFSoC supports this feature by applying MTS with a targeted delay which is simply an optional user parameter of the MTS algorithm. This targeted latency value is expressed in a multiple of T1 and can be extracted by MTS process report itself. It should then be applied with a small margin as explained in the Zynq UltraScale+ RFSoC product guide. The main principle here is to force the algorithm with a fixed delay target which the system can achieve in the MTS process.

To achieve strict deterministic latency over multiple chips, as mentioned in Dual Clock FIFO section, the analog_sysref and PL_clock signal groups must keep constant phase relationship over reset to reset cycles.

Practical Application of MTS

Once the hardware requirements detailed above for Sysref and clocking are met, there are two API functions required to perform MTS on a device. The first, `XRFdc_MultiConverter_Init` is used to setup which tiles are to be synchronized and from Vivado Release 2021.1. The second is the reference tile, which is used as the basis for calculating latency mismatch across FIFOs.

As part of the MTS process, Sysref is distributed to each tile and scanned by each sampling clock period (T1) in use in the clock system of the targeted tile set. This ensures RFDC sub-system can safely capture Sysref on each RFDC tile. In first and second generation of RFSoC devices, all sampling clocks of tile set were required to be scanned when in use. RFSoC Gen3 provides the ability to forward clocks using the on-chip clock distribution, there are multiple clock distribution scenarios which mean that only a subset of available tiles need to be scanned in a device. In general, when using on-chip clock forwarding feature, you should set the sampling clock source tile which is distributing the clock as the reference tile. In first and second generation of RFSoC devices, the reference tile parameter can be left at the default value of 0.

The MTS process can then be completed using the second API function `XRFdc_MultiConverter_Sync`. This API function will distribute sysref signal to each tile, determine the optimal capture code and align FIFOs to achieve synchronization across tiles. Refer to *Zynq UltraScale+ RFSoC RF Data Converter LogiCORE IP Product Guide* (PG269) for details.

When this is complete, the metal log can be viewed to check the procedure to capture Sysref on both the analog and PL side completed as expected and that FIFO alignment has also been achieved. This will also provide debug information in the case where MTS is not functioning as expected.

An example of a typical metal log for the case where we are distributing a sampling clock using on-chip RF-PLL from ADC Tile 2 to all other ADC Tiles using a ZU48DR device is shown below (DTC scan codes are incomplete).

```
Info:
DTC Scan PLL
Info: ADC2:
1322000000000001132200000000001113220000000000111222000 0*0000011#2220000000
Info:
DTC Scan T1
Info: ADC2:
000000000000000000000000000000001113222000000000000000000000000#0*00000000
Info: ADC0:
000000000000000000000000000000113222000000000000000000000000000*00#00000000
Info: ADC1:
000000000000000000000000000000113222000000000000000000000000000*#00000000
Info: ADC3:
000000000000000000000000000000111222200000000000000000000000000#*0000000
Info: ADC0: Marker: - 9, 8
Info: ADC1: Marker: - 10, 4
Info: ADC2: Marker: - 10, 4
Info: ADC3: Marker: - 10, 4
Info: SysRef period in terms of ADC T1s = 384
Info: ADC target latency = 116
```

As can be seen in the log, the DTC (Delay Tap Chain) scan on the Sysref, is only performed for the PLL in ADC2. The 0's in each scan represent a safe area in which to sample Sysref and the 1's, 2's and 3's represent the Sysref edge as scanned in the DTC. The # represents the starting scan point and is always set to tap 64 out of 128 for the reference tile. The * represents the safe sampling point determined by the scan. This is used as the starting point for subsequent tiles.

In the above example, lengths of chains of 1's, 2's and 3's are fine. Longer chains of 1's, 2's and 3's in the scan can indicate too much jitter is present on the Sysref capture, it will error out with DTC scan failed. If a reliable sampling point cannot be attained, MTS cannot perform effectively.

After the DTC scan, information on the marker counter value and the location of the marker in the FIFO is shown. Referring to the log above and for ADC0, the marker counter value is 9 and the marker location is word 8. The marker counter values should be reasonably close in value for each tile and the marker location should be within the width of the FIFO. For example, if the FIFO width is set to 12, then a marker location of 14 indicates that the FIFO may be in under/overflow or that there is an issue with the PL clocking setup which warrants further investigation.

The Sysref period is reported in terms of T1's. Incorrect values here can indicate an issue capturing Sysref in the PL. Ensure all clocking requirements are met and the recommended Sysref capture scheme is utilized as detailed in *Zynq UltraScale+ RFSoC RF Data Converter LogiCORE IP Product Guide* (PG269).

Finally, the ADC/DAC target latency is reported which is the maximum latency through the tiles after FIFO adjustments have been made. A small piece of code can be added to report latencies and adjustments made for all tiles.

```
// Report Overall Latency in T1 (Sample Clocks) and Offsets (in terms of PL
words) added to each FIFO
metal_log(METAL_LOG_INFO,"\n=== Multi-Tile Sync Report ===\n\n");
for(i=0; i<4; i++) {
    if((1<<i)&DAC_Sync_Config.Tiles) {
        XRFdc_GetInterpolationFactor(RFdcInstPtr, i, 0, &factor);
        metal_log(METAL_LOG_INFO,"  DAC%d: Latency(T1) =%3d, Adjusted Delay
Offset(T%d) =%3d\n", i, DAC_Sync_Config.Latency[i], factor,
DAC_Sync_Config.Offset[i]);
        }
}
for(i=0; i<4; i++) {
    if((1<<i)&ADC_Sync_Config.Tiles) {
        XRFdc_GetDecimationFactor(RFdcInstPtr, i, 0, &factor);
        metal_log(METAL_LOG_INFO,"  ADC%d: Latency(T1) =%3d, Adjusted Delay
Offset(T%d) =%3d\n", i, ADC_Sync_Config.Latency[i], factor,
ADC_Sync_Config.Offset[i]);
        }
}
```

```
Info: ADC0: Latency(T1) = 116, Adjusted DelayOffset(T1) = 8
Info: ADC1: Latency(T1) = 116, Adjusted DelayOffset(T1) = 0
Info: ADC2: Latency(T1) = 116, Adjusted DelayOffset(T1) = 0
Info: ADC3: Latency(T1) = 116, Adjusted DelayOffset(T1) = 0
```

It is important to note that latency here refers to latency through the FIFO relative to when analog Sysref and Digital Sysref are detected at either side of the FIFO and is not a true representation of latency through the tile.

Lab Measurements

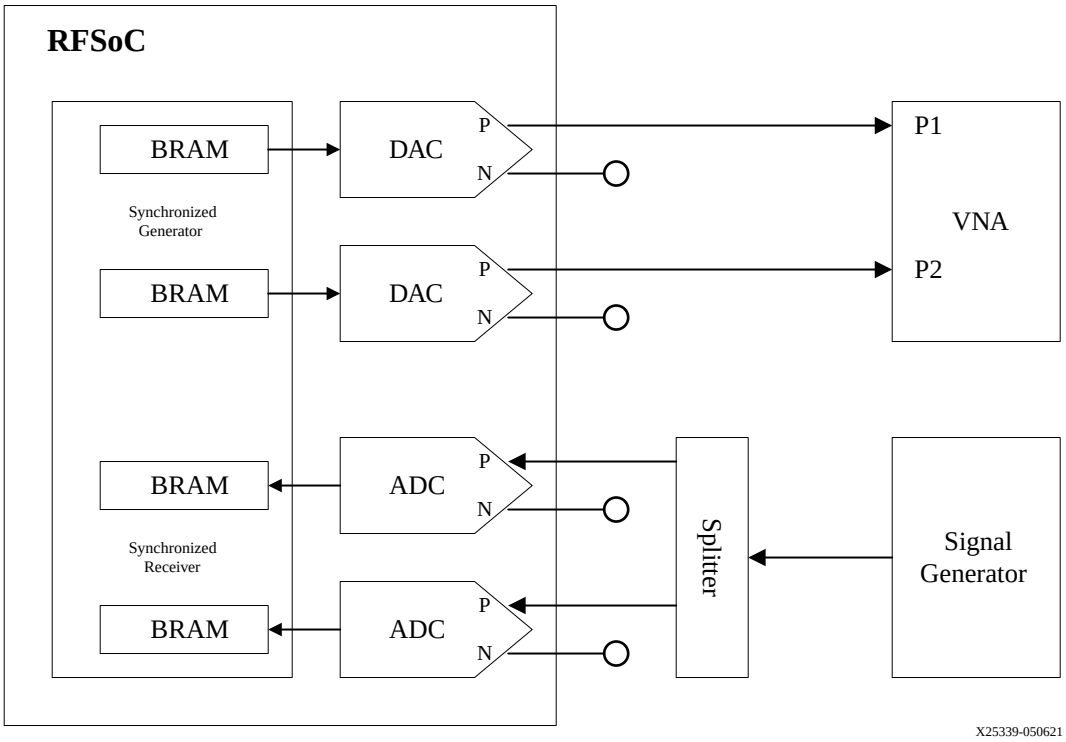
The phase difference of multiple converter channels can be derived from their phase spectrum in frequency domain when input or output CW signals.

Measurement Setup

In the lab, the VNA (Vector Network Analyzer) is used to measure alignment of multiple RF-DACs. Multiple RF-DAC channels are synchronized and output CW signals at the same frequency, VNA is configured in receiver mode, to capture the input CW signal and calculate the phase difference between ports in frequency domain. The results are showed as phase difference between one reference channel versus all other channels. For ADC, the same theory applies, CW signals from a multi-ports power splitter were fed into multiple RF-ADC channels, all these RF-ADC channels have been synchronized, data are captured at the same time, then FFT analysis will give the phase difference on each channel versus a reference channel.

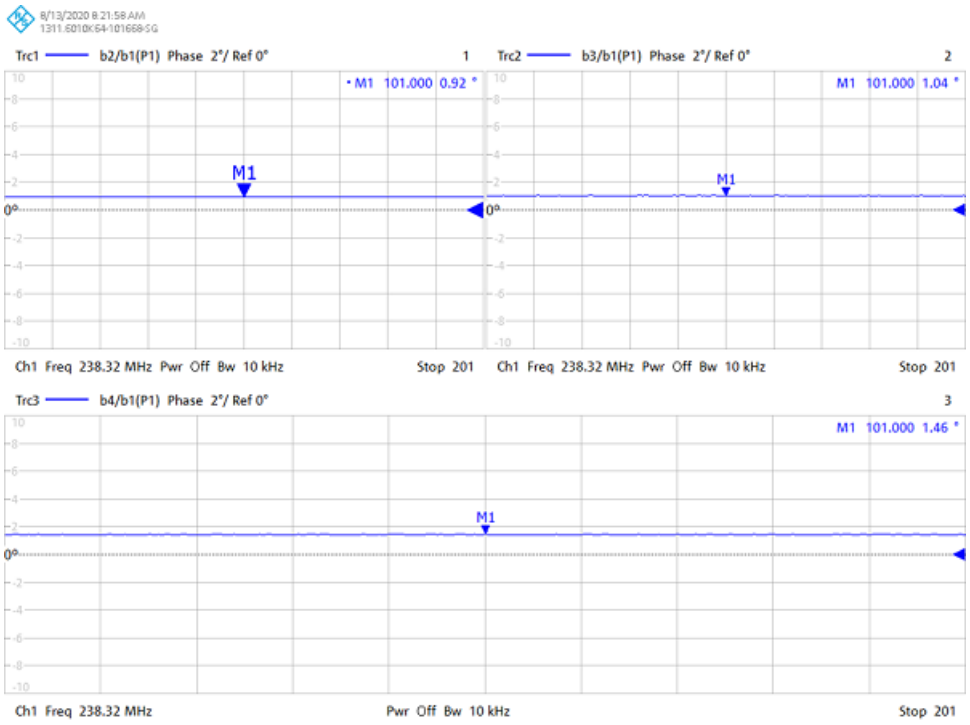
Based on previous discussion in this application notes, the PCB should be well designed to match the trace of each converter channels and related clock signals, the ZCU1275 V2.0 verification board is used for measurements, other accessories such as cables, power splitter are also carefully picked up to avoid misalignment. In the testing the baluns are not used to avoid introducing potential phase imbalance. For both ADCs and DACs, only P legs were used for signal inputs and outputs, the N legs were 50Ω terminated. The following figure illustrates the set up.

Figure 8: **MTS Measurement Set Up**



A capture of VNA is showed as following for example, the phase difference of three RF-DAC channels versus one reference channel are measured.

Figure 9: **Phase Difference in VNA**



MTS Results

The phase difference of each tile versus reference tile (tile 0 used in this measurement) has been measured under the combination of different temperatures, voltage supplies, manufacturing process corners and clock scheme. Measurements showed excellent alignment across multiple tiles on ZU49DR, and the alignment is almost independent over temperature and voltage, and also proved that sampling clock distribution is better than reference clock distribution as we mentioned in previous section. For the tests clock forwarding feature was used to distribute either the external sampling clock (0-PLL), internal PLL RF sampling clock(1-PLL) or the internal PLL reference clock to multiple PLLs (4-PLLs). Figure 10 gives an example, refer to the characterization report for detailed results.

Figure 10: **ADC MTS Min/Max Values**

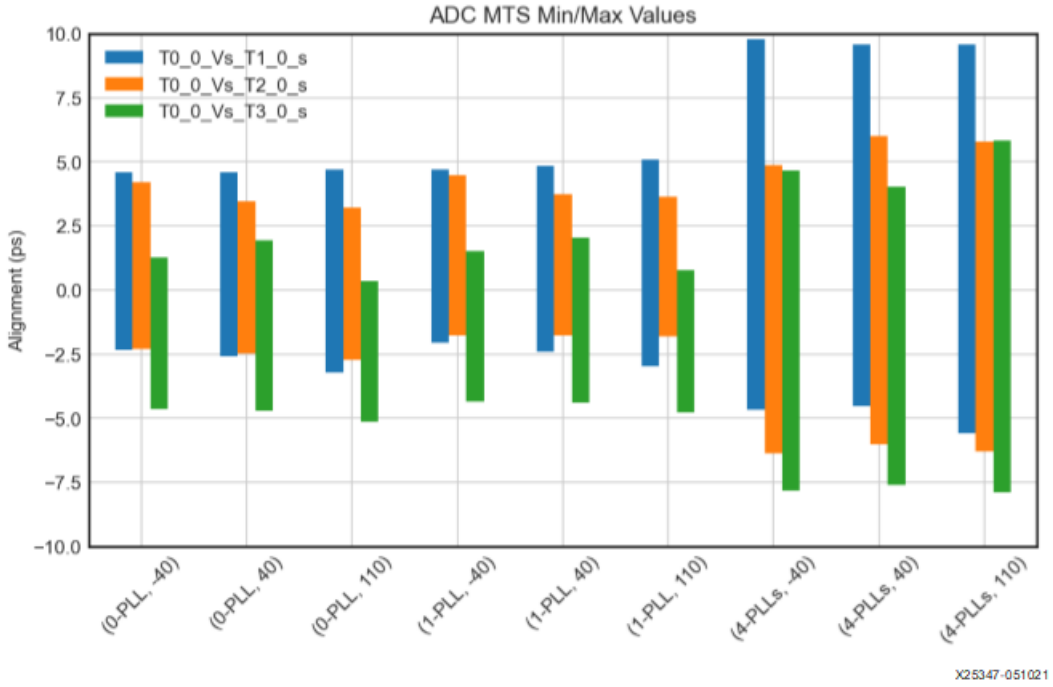
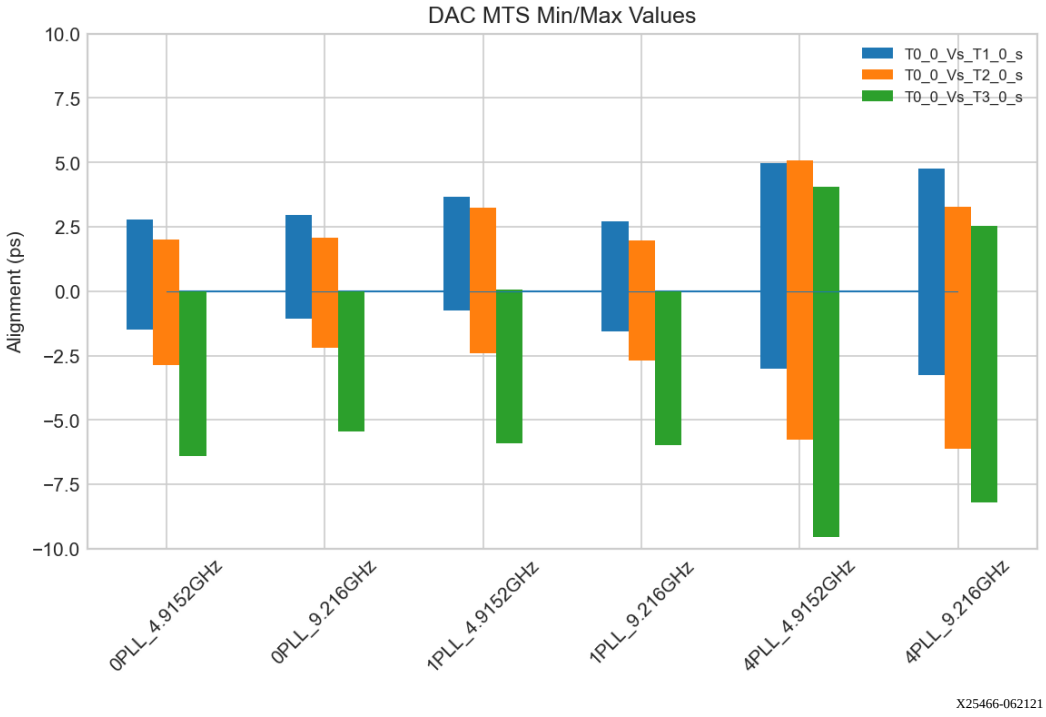


Figure 10 gives the minimum and maximum alignments of RF-ADC tiles in lab measurements, over different clock distribution schemes and temperatures. Measurement showed the alignment varies little over temperature from -40 to 110 degrees. the 4-PLL clock scheme (reference clock forwarding to each tile and generate sample clock by in-tile PLLs) showed the biggest spread over 0-PLL (distribute external sample clock) and 1-PLL (distribute sample clock generated by one in-tile PLL) clock schemes. Results also demonstrate that there is very little difference in MTS alignment performance between using the distributed internal PLL and the distributed external RF sampling clock.

The following figure shows similar measurement results of RF-DAC tiles.

Figure 11: **DAC MTS Min/Max values**



Conclusion

We go through the potential sources in a system which impact the synchronization across RF channels using different clocking system to sample data. The following summary gives some notes for optimized alignment across multiple chips:

1. There are four key clocks groups: sample clock group (RF-ADCs and RF-DACs), PL_clock group, analog_sysref group and PL_sysref group; the clocks should be well aligned each other's within their clock groups.
2. The phase relationship between these four groups must be fixed over reset to reset cycles to ensure determinism.

Comparing with the JESD-204B/C interface, the sampling clock and PL_clock groups are similar to the device clocks group, and the PL_sysref and analog_sysref groups are like the sysref group, although the requirements are easier to meet with the Zynq UltraScale+ RFSoC compared to JESD-204B/C.

1. Clock PCB trace mismatches introduce misalignment directly on RF paths and misalignment can be corrected by MTS algorithm in most of the cases. To align the length of traces on above key clock signals is a good practice to achieve the optimized synchronization.
2. Using well aligned external sampling clock directly instead of multiple on-chip RF PLLs will achieve better alignment performance
3. The skew of external clock generator and clock buffer need to be considered for the best MTS accuracy performance.

The above are general requirements for most multiple channel system who need synchronization.

Finally, the on-chip clock distribution network reduces the number of external clock routing and helps to align these clock traces inside the chip. This use of the on-chip clock forwarding can give the best trace alignments between channels tile usage when well balanced, see *Zynq UltraScale+ RFSoC RF Data Converter LogiCORE IP Product Guide* (PG269) for application details of clock forwarding in the third generation of Zynq UltraScale+ RFSoC. The higher channel density the chip will get, the smaller number of clocks on board need to meet strict constraints.

References

These documents provide supplemental material useful with this guide:

1. Zynq® UltraScale+™ RFSoC RFDC
2. *Zynq UltraScale+ RFSoC RF Data Converter LogiCORE IP Product Guide* (PG269)
3. *UltraScale Architecture PCB Design User Guide* (UG583)
4. *Zynq UltraScale+ RFSoC Data Sheet: DC and AC Switching Characteristics* (DS926)

Revision History

The following table shows the revision history for this document.

Section	Revision Summary
2/17/2022 Version 1.0	
Initial Xilinx release.	N/A

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